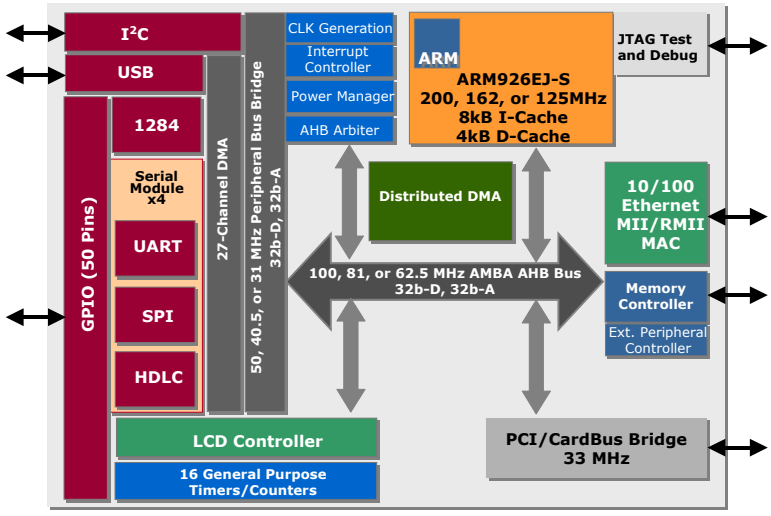
NetSilicon
A Digi International® Company

NS9750 Datasheet

The NetSilicon® NS9750 is a single chip 0.13µm CMOS network-attached processor. The CPU is the ARM926EJ-S core with MMU, DSP extensions, Jazelle Java accelerator, and 8 kB of instruction cache and 4 kB of data cache in a Harvard architecture. NS9750 runs up to 200 MHz, with a 100 MHz system and memory bus and 50 MHz peripheral bus. NS9750 operates at a 1.5V core and 3.3V I/O ring voltages.



With its extensive set of I/O interfaces, Ethernet high-speed performance and processing capacity, NS9750 is the most capable of highly integrated 32-bit network-attached processors available. NS9750 is designed specifically for use in high-performance intelligent networked devices and Internet appliances including high-performance/low-latency remote I/O, intelligent networked information displays, and streaming and surveillance cameras. The NS9750 is a member of the award-winning NET+ARM family of system-on-chip (SOC) solutions for embedded systems.

NS9750 offers a connection to an external bus expansion module as well as a glueless connection to SDRAM, PC100 DIMM, Flash, EEPROM, and SRAM memories, and an

external bus expansion module. It includes a versatile embedded LCD controller supporting up to 16M color TFT or 3375 color STN. NS9750 features a PCI/CardBus port as well as a USB port for applications requiring WLAN, external storage, or external sensors, imagers, or scanners. Four multi-function serial ports, an I^2C port, and 1284 parallel port provide a standard glueless interface to a variety of external peripherals. NS9750 features up to 50 general purpose I/O (GPIO) pins and highly-configurable power management with sleep mode.

NET+ARM processors are the foundation for the NET+Works® family of integrated hardware and software solutions for device networking. These comprehensive platforms include drivers, operating systems, networking software, development tools, APIs, and complete development boards.

Using NS9750 and associated Net+Works packages allows system designers to achieve dramatic time-to-market reductions with pre-integrated and tested NET+ARM hardware, NET+Works software, and tools. Product unit costs are reduced dramatically with complete system-on-chip, including Ethernet, display support, a robust peripheral set, and the processing headroom to meet the most demanding applications. Customers save engineering resources, as no network development is required. Companies will reduce their design risk with a fully integrated and tested solution.

A complete NET+Works development package includes ThreadX™ picokernel RTOS, Green Hills™ MULTI® 2000 IDE or Microcross GNU X-Tools™, drivers, networking protocols and services with APIs, NET+ARM-based development board, NetSilicon-supplied utilities, Integrated File System, JTAG In Circuit Emulator (ICE), and support for Boundary Scan Description Language (BSDL). One year software maintenance and technical support is available.

Contents

NS9750 Features

32-bit ARM926EJ-S RISC processor

- 125 to 200 MHz
- 5-stage pipeline with interlocking
- Harvard architecture
- 8 kB instruction cache and 4 kB data cache
- 32-bit ARM and 16-bit Thumb instruction sets. Can be mixed for performance/code density tradeoffs
- MMU to support virtual memory-based OSs such as Linux, WinCE/Pocket PC, VxWorks, others
- DSP instruction extensions, improved divide, single cycle MAC
- ARM Jazelle, 1200CM (coffee marks) Java accelerator
- EmbeddedICE-RT debug unit
- JTAG boundary scan, BSDL support

External system bus interface

- 32-bit data, 32-bit internal address bus, 28-bit external address bus
- Glueless interface to SDRAM, SRAM, EEPROM, buffered DIMM, Flash
- 4 static and 4 dynamic memory chip selects
- 0–63 wait states per chip select
- Self-refresh during system sleep mode
- Automatic dynamic bus sizing to 8 bits, 16 bits, 32 bits
- Burst mode support with automatic data width adjustment
- Two external DMA channels for external peripheral support

System Boot

- High-speed boot from 8-bit, 16-bit, or 32-bit ROM or Flash
- Hardware-supported low cost boot from serial EEPROM through SPI port (patent pending)

High performance 10/100 Ethernet MAC

- 10/100 Mbps MII/RMII PHY interfaces
- Full-duplex or half-duplex
- Station, broadcast, or multicast address filtering
- 2 kB RX FIFO
- 256 byte Tx FIFO with on-chip buffer descriptor ring
  - Eliminates underruns and decreases bus traffic
- Separate Tx and Rx DMA channels
- Intelligent receive-side buffer size selection
- Full statistics gathering support
- External CAM filtering support

PCI/CardBus port

- PCI v2.2, 32-bit bus, up to 33 MHz bus speed
- Programmable to:
  - PCI device mode
  - PCI host mode:
    Supports up to 3 external PCI devices
    Embedded PCI arbiter or external arbiter
- CardBus host mode

Flexible LCD controller

- Supports most commercially available displays:
  - Active Matrix color TFT displays
    Up to 24bpp direct 8:8:8 RGB; 16M colors
  - Single and dual panel color STN displays:
    Up to 16bpp 4:4:4 RGB; 3375 colors
  - Single and dual-panel monochrome STN displays
    1, 2,4bpp palettized gray scale
- Formats image data and generates timing control signals
- Internal programmable palette LUT and grayscaler support different color techniques
- Programmable panel-clock frequency

USB ports

- USB v.2.0 full speed (12 Mbps) and low speed (1.5 Mbps)
- Configurable to device or OHCI host
  - USB host is bus master
  - USB device supports one bidirectional control endpoint and 11 unidirectional endpoints
- All endpoints supported by a dedicated DMA channel; 13 channels total
- 20 byte Rx FIFO and 20 byte Tx FIFO

Serial ports

- 4 serial modules, each independently configurable to UART mode, HDLC mode, SPI master mode, or SPI slave mode
- Bit rates from 75 bps to 921.6 kbps: asynchronous x16 mode
- Bit rates from 1.2 kbps to 6.25 Mbps: synchronous mode
- UART provides:
  - High-performance hardware and software flow control
  - Odd, even, or no parity
  - 5, 6, 7, or 8 bits
  - 1 or 2 stop bits
  - Receive-side character and buffer gap timers

- Internal or external clock support, digital PLL for Rx clock extraction
- 4 receive-side data match detectors
- 2 dedicated DMA channels per module, 8 channels total
- 32 byte Tx FIFO and 32 byte Rx FIFO per module

I²C port

- I²C v.1.0, configurable to master or slave mode
- Bit rates: fast (400 kHz) or normal (100 kHz) with clock stretching
- 7-bit and 10-bit address modes
- Supports I²C bus arbitration

1284 parallel peripheral port

- All standard modes: ECP, byte, nibble, compatibility (also known as SPP or "Centronix")
- RLE (run length encoding) decoding of compressed data in ECP mode
- Operating clock from 100 kHz to 2 MHz

High performance multiple-master/distributed DMA system

- Intelligent bus bandwidth allocation (patent pending)
- System bus and peripheral bus

System bus:

- Every system bus peripheral is a bus master with a dedicated DMA engine

Peripheral bus:

- One 13-channel DMA engine supports USB device
  - 2 DMA channels support control endpoint
  - 11 DMA channels support 11 endpoints
- One 12-channel DMA engine supports:
  - 4 serial modules (8 DMA channels)
  - 1284 parallel port (4 DMA channels)
- All DMA channels support fly-by mode

External peripheral:

- One 2-channel DMA engine supports external peripheral connected to memory bus
- Each DMA channel supports memory-to-memory transfers

Power management (patent pending)

- Power save during normal operation
  - Disables unused modules
- Power save during sleep mode
  - Sets memory controller to refresh
  - Disables all modules except selected wakeup modules
  - Wakeup on valid packets or characters

Vector interrupt controller

- Decreased bus traffic and rapid interrupt service
- Hardware interrupt prioritization

General purpose timers/counters

- 16 independent 16-bit or 32-bit programmable timers or counters
  - Each with an I/O pin
- Mode selectable into:
  - Internal timer mode
  - External gated timer mode
  - External event counter
- Can be concatenated
- Resolution to measure minute-range events
- Source clock selectable: internal clock or external pulse event
- Each can be individually enabled/disabled

System timers

- Watchdog timer
- System bus monitor timer
- System bus arbiter timer
- Peripheral bus monitor timer

General purpose I/O

- 50 programmable GPIO pins (muxed with other functions)
- Software-readable powerup status registers for every pin for customer-defined bootstrapping

External interrupts

- 4 external programmable interrupts
  - Rising or falling edge-sensitive
  - Low level- or high level-sensitive

Clock generator

- Low cost external crystal
- On-chip phase locked loop (PLL)
- Software programmable PLL parameters
- Optional external oscillator
- Separate PLL for USB

Operating grades/Ambient temperatures

- 200 MHz: 0 – 70° C
- 162 MHz: -40 – +85° C
- 125 MHz: 0 – 70° C

System-level interfaces

Figure 1 shows the NS9750 system-level hardware interfaces, which are further detailed after the figure.

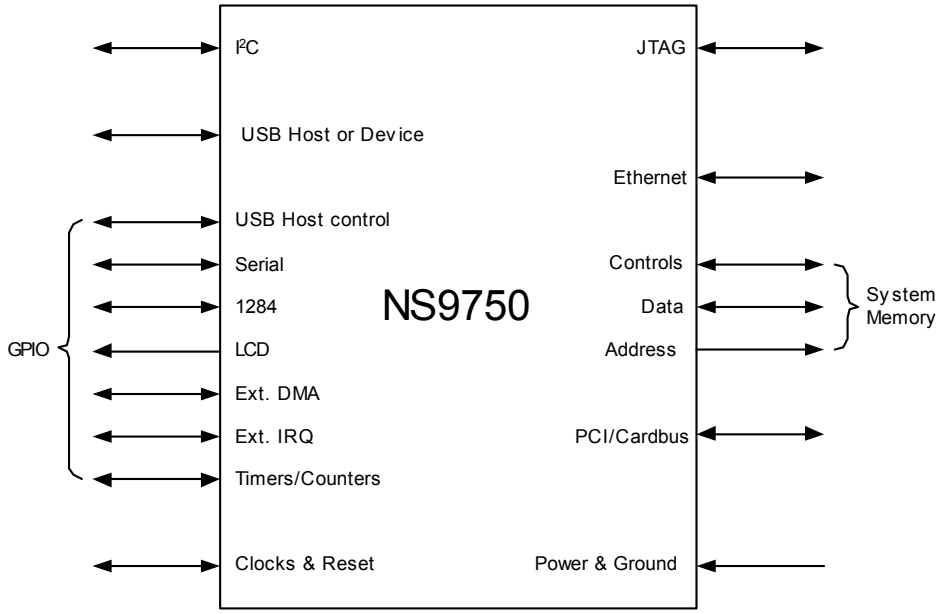


Figure 1: System-level hardware interfaces

NS9750 interfaces

- Ethernet MII/RMII interface to an external PHY
- System Memory interface
  - Glueless connection to SDRAM
  - Glueless connection to buffered PC100 DIMM
  - Glueless connection to SRAM
  - Glueless connection to Flash memory or ROM
- PCI muxed with CardBus interface
- USB Host or Device interface
- I^2C interface
- 50 GPIO pins muxed with:
  - Four 8-pin-each serial ports, each programmable to UART, SPI, or HDLC
  - 1284 port
  - Up to 24-bit TFT or STN color and monochrome LCD controller
  - Two external DMA channels
  - Four external interrupt pins programmed to rising or falling edge, or to high or low level

  - Sixteen 16-bit or 32-bit programmable timers or counters
  - Two control signals to support USB host
- JTAG development interface
- Clock interfaces for crystal or external oscillator
  - System clock
  - USB clock
- Clock interface for optional LCD external oscillator
- Power and ground

System configuration

The PLL and other system settings can be configured at powerup before the CPU boots. External pins configure the necessary control register bits at powerup. Internal pullup resistors on the external pins provide a default configuration. Weak external pulldown resistors can be used to configure the PLL and system configuration registers depending on the application.

Table 1 indicates how each bit is used to configure the powerup settings.

Pin name	Configuration bits
rtck	**PCI arbiter configuration** 0 External PCI arbiter 1 Internal PCI arbiter (default) This bit is not inverted.
boot_strap[0]	**Chip select 1 byte lane enable polarity bootstrap select** 0 Active low (default) 1 Active high This signal is inverted to produce a default configuration of `1'b0`, active low.
boot_strap[4:3]	**Chip select 1 data width bootstrap select** `boot_strap[3]` is inverted and `boot_strap[4]` is not inverted, to produce a default configuration of `2'b10`, which is 32 bits wide. The range of settings is: 00 8 bits 01 16 bits 10 32 bits (default)
boot_strap[2]	**Memory interface read mode bootstrap select** 0 Command delayed mode Commands are launched on a 90-degree phase-shifted AHB clock, and AHB clock is routed to the external dynamic memory. 1 Clock delayed mode Commands are launched on AHB clock and a 90-degree phase-shifted AHB clock is routed to the dynamic memory (default).
boot_strap[1]	**CardBus mode bootstrap select** 0 CardBus mode 1 PCI mode (default)
gpio[49]	**Chip select polarity** 0 Active low (default) 1 Active high This bit is inverted.
gpio[44]	**Endian mode** 0 Little Endian (default) 1 Big Endian This bit is inverted.

Table 1: Configuration pins— Bootstrap initialization

Pin name	Configuration bits
reset_done	**Bootup mode** 0 Boot from SDRAM using serial SPI EEPROM 1 Boot from flash/ROM (default) This bit is not inverted.
gpio[24], gpio[20]	**PLL IS[1:0] (PLL charge pump current control)** These bits are not inverted, such that the default setting is `2'b11`. The recommended settings are determined by ND, as shown: IS ND 00 0–3 01 4–7 10 8–15 11 16–31 (default)
gpio[19]	**PLL BP (PLL bypass)** 0 PLL not bypassed (default) 1 PLL bypassed This bit is inverted such that the PLL is not bypassed in the default mode.
gpio[17], gpio[12], gpio[10], gpio [8], gpio[4]	**PLL ND[4:0] (PLL multiplier, ND + 1)** Bits gpio[10] and gpio[4] are inverted to produce a default configuration of `5'b11010` or 26. This gives a default PLL multiplier factor of 27.
gpio[2], gpio[0]	**PLL FS[1:0] (PLL frequency select)** These inputs are inverted such that the `2'b11` default setting produces a `2'b00` configuration.

Table 1: Configuration pins— Bootstrap initialization

There are 32 additional GPIO pins that are used to create a general purpose, user-defined ID register. These are external signals that are registered at powerup.

gpio[41]	gpio[40]	gpio[39]	gpio[38]
gpio[37]	gpio[36]	gpio[35]	gpio[34]
gpio[33]	gpio[32]	gpio[31]	gpio[30]
gpio[29]	gpio[28]	gpio[27]	gpio[26]
gpio[25]	gpio[23]	gpio[22]	gpio[21]
gpio[18]	gpio[16]	gpio[15]	gpio[14]
gpio[13]	gpio[11]	gpio[9]	gpio[7]
gpio[6]	gpio[5]	gpio[3]	gpio[1]

Read these signals for general purpose status information.

System boot

There are two ways to boot the NS9750 system (see Figure 2, "Two methods of booting NS9750 system," on page 7):

- From a fast Flash over the system memory bus
- From an inexpensive, but slower, serial EEPROM through SPI port A. Both boot methods are glueless. The bootstrap pin, `RESET_DONEn`, is used to indicate where to boot on a system powerup.

Flash boot can be done from 8-bit, 16-bit, or 32-bit ROM or Flash.

Serial EEPROM boot is supported by NS9750 hardware. A configuration header in the EEPROM specifies total number of words to be fetched from EEPROM, as well as a system memory configuration and a memory controller configuration. The boot engine configures the memory controller and system memory, fetches data from low-cost serial EEPROM, and writes the data to external system memory, holding the CPU in reset.

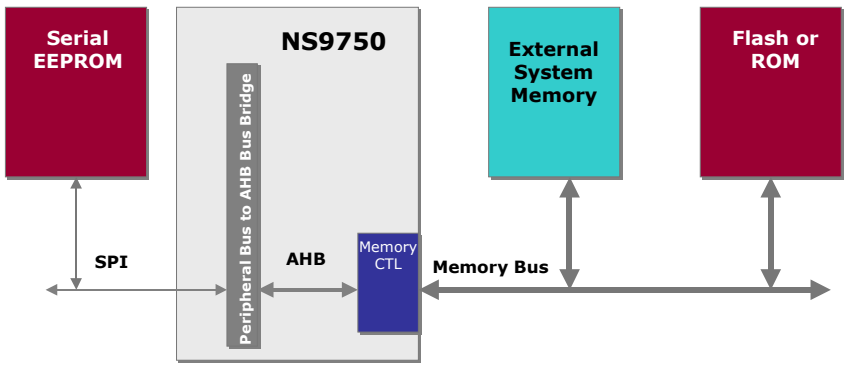


Figure 2: Two methods of booting NS9750 system

Reset

Master reset using an external reset pin resets NS9750. Only the AHB bus error status registers retain their values; software read resets these error status registers. The input reset pin can be driven by a system reset circuit or a simple poweron reset circuit.

RESET_DONE as an input

Used at bootup only:

- When set to 0, the system boots from SDRAM through the serial SPI EEPROM.
- When set to 1, the system boots from Flash/ROM. This is the default.

RESET_DONE as an output

Sets to 1, per Step 6 in the boot sequence:

If the system is booting from serial EEPROM through the SPI port, the boot program must be loaded into the SDRAM before the CPU is released from reset. The Memory controller is powered up with `dy_cs_n[0]` enabled with a default set of SDRAM configurations. The default address range for `dy_cs_n[0]` is from `0x0000 0000`. The other chip selects are disabled.

Boot sequence

1. When the system reset turns to inactive, the reset signal to the CPU is still held active.
2. An I/O module on the peripheral bus (BBus) reads from a serial ROM device that contains the memory controller settings and the boot program.
3. The BBus-to-AHB bridge requests and gets the system bus.
4. The memory controller settings are read from the serial EEPROM and used to initialize the memory controller.
5. The BBus-to-AHB bridge loads the boot program into the SDRAM, starting at address 0.
6. The reset signal going to the CPU is released once the boot program is loaded. `RESET_DONE` is now set to 1.
7. The CPU begins to execute code from address `0x0000 0000`.

Figure 3 shows a sample reset circuit.

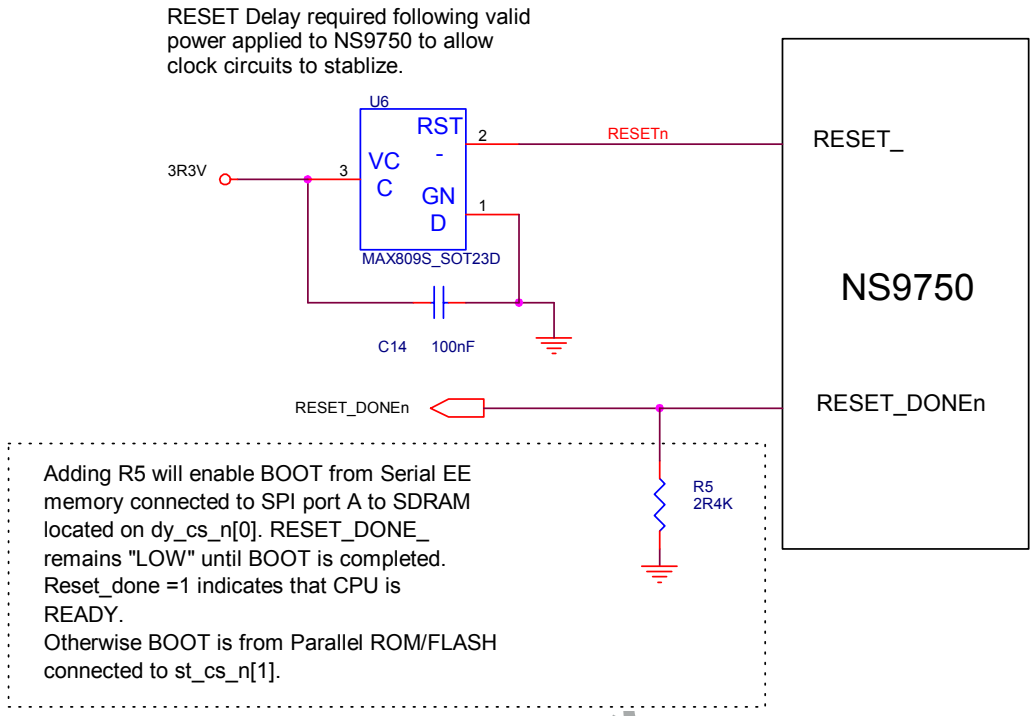


Figure 3: Sample reset circuit

You can use one of four software resets to reset NS9750. Select the reset by setting the appropriate bit in the appropriate register:

- Watchdog timer can issue reset upon Watchdog timer expiration.
- AHB bus arbiter can issue reset upon AHB bus arbiter timer expiration.
- AHB bus monitor can issue reset upon AHB bus monitor timer expiration.
- Software reset can reset individual internal modules or all modules (except memory and CPU).

Hardware reset duration is 4ms for PLL to stabilize. Software reset duration depends on speed grade, as shown in Table 2.

Speed grade	CPU clock cycles	Duration
200 MHz	128	640 ns
162 MHz	128	790 ns
125 MHz	128	1024 ns

Table 2: Software reset duration

The minimum reset pulse width is 10 crystal clocks.

System Clock

The system clock is provided to NS9750 by either a crystal or an external oscillator; Table 3 shows sample clock frequency settings for each chip speed grade.

Speed	cpu_clk	hclk (main bus)	bbus_clk
200 MHz	200 (199.0656)	99.5328	49.7664
162 MHz	162.2016	81.1008	40.5504
125 MHz	125.3376	62.6688	31.3344

Table 3: Sample clock frequency settings with 14.7456 MHz crystal

If an oscillator is used, it must be connected to the `x1_sys_osc` input (C8 pin) on the NS9750. If a crystal is used, it must be connected with a circuit such as the one shown in Figure 4.

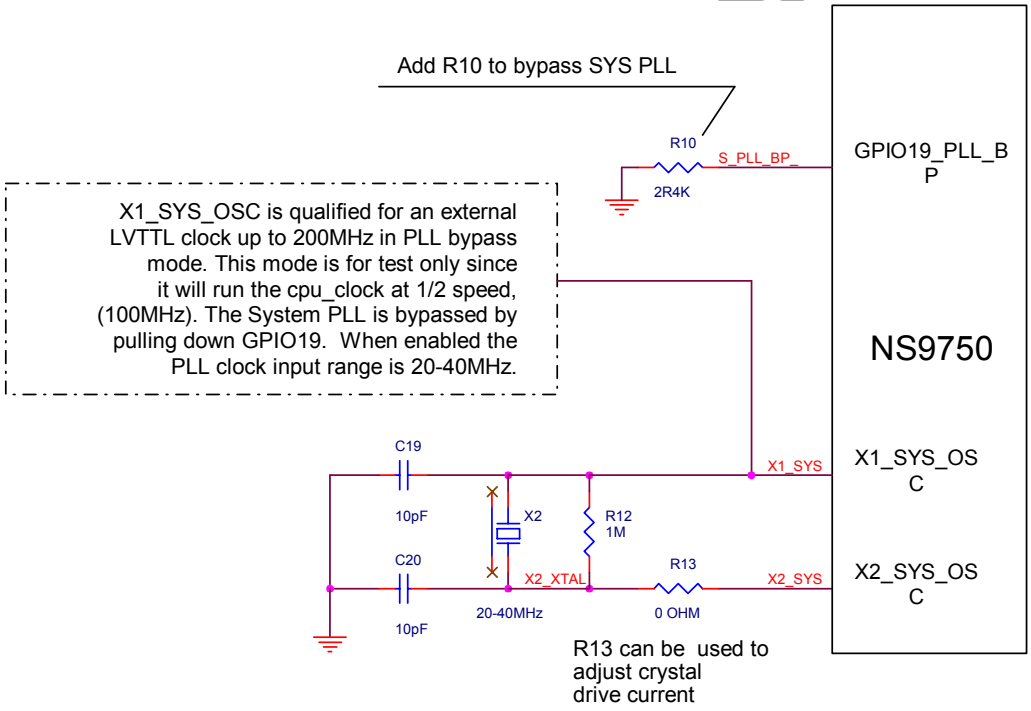


Figure 4: NS9750 system clock

The PLL parameters are initialized on powerup reset, and can be changed by software from f_{max} to $1/2\ f_{max}$. For a 200MHz grade, then, the CPU may change from 200 MHz to 100 MHz, the AHB system bus may change from 100 MHz to 50 MHz, and the peripheral BBus may change from 50 MHz to 25 MHz. If changed by software, the system resets automatically after the PLL stabilizes (approximately 4 ms).

The system clock provides clocks for CPU, AHB system bus, peripheral BBus, PCI/CardBus, LCD, timers, memory controller, and BBus modules (serial modules and 1284 parallel port).

The Ethernet MAC uses external clocks from a MII PHY or a RMII PHY. For a MII PHY, these clocks are input signals: `rx_clk` on pin T3 for receive clock and `tx_clk` on pin V3 for transmit clock. For a RMII, there is only one clock, and it connects to the `rx_clk` on pin T3. In this case, the transmit clock `tx_clk`, pin V3, should be tied low.

PCI/CardBus, LCD controller, serial modules (UART, SPI HDLC), and 1284 port optionally can use external clock signals.

USB clock

USB is clocked by a separate PLL driven by an external 48 MHz crystal, or it can be driven directly by an external 48 MHz oscillator. Figure 5 shows a USB circuit.

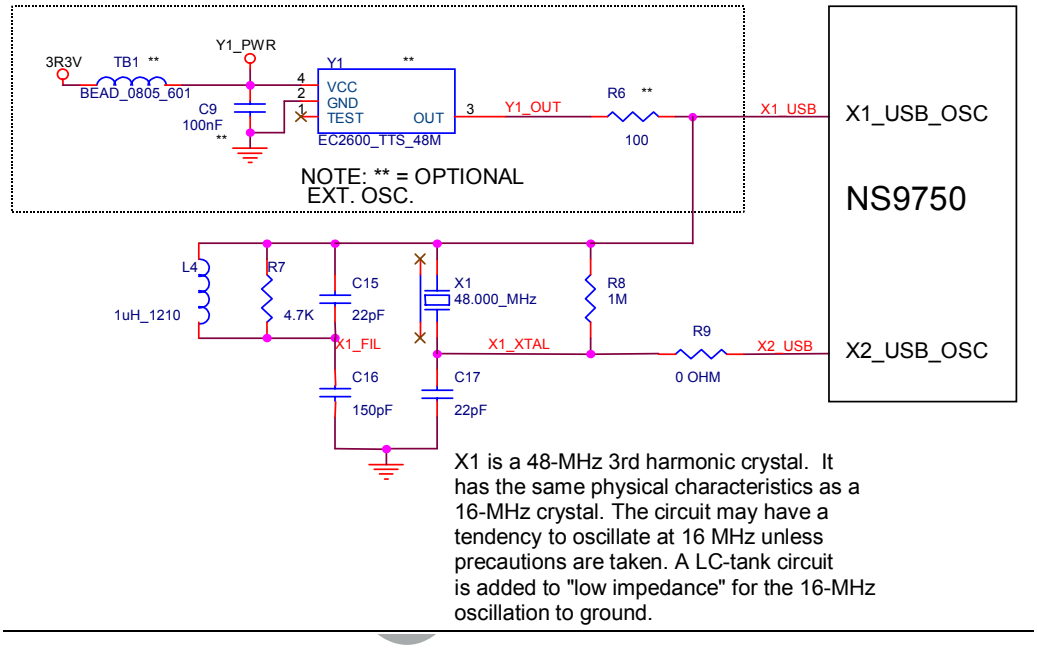


Figure 5: USB clock

NS9750 pinout and signal descriptions

Each pinout table applies to a specific interface, and contains the following information:

Heading	Description
Pin #	The pin number assignment for a specific I/O signal.
Signal	The pin name for each I/O signal.Some signals have multiple function modes and are identified accordingly. The mode is configured through firmware using one or more configuration registers. _n in the signal name indicates that this signal is active *low*.
U/D	U or D indicates whether the pin is a pullup resistor or a pulldown resistor: ■ **U** — Pullup (input current source) ■ **D** — Pulldown (input current sink) If no value appears, that pin is neither a pullup nor pulldown resistor.
I/O	The type of signal — input, output, or input/output (I/O).
OD (mA)	The output drive strength of an output buffer. The NS9750 uses one of three drivers: ■ 2 mA ■ 4 mA ■ 8 mA

More detailed signal descriptions are provided for selected modules.

System Memory interface

Pin #	Signal Name	U/D	OD (mA)	I/O	Description
A21	addr[0]		8	O	Address bus signal
B20	addr[1]		8	O	Address bus signal
C19	addr[2]		8	O	Address bus signal
A20	addr[3]		8	O	Address bus signal
B19	addr[4]		8	O	Address bus signal
C18	addr[5]		8	O	Address bus signal
A19	addr[6]		8	O	Address bus signal
A17	addr[7]		8	O	Address bus signal
C16	addr[8]		8	O	Address bus signal
B16	addr[9]		8	O	Address bus signal
A16	addr[10]		8	O	Address bus signal
D15	addr[11]		8	O	Address bus signal

Table 4: System Memory interface pinout

Pin #	Signal Name	U/D	OD (mA)	I/O	Description
C15	addr[12]		8	O	Address bus signal
B15	addr[13]		8	O	Address bus signal
A15	addr[14]		8	O	Address bus signal
C14	addr[15]		8	O	Address bus signal
B14	addr[16]		8	O	Address bus signal
A14	addr[17]		8	O	Address bus signal
A13	addr[18]		8	O	Address bus signal
B13	addr[19]		8	O	Address bus signal
C13	addr[20]		8	O	Address bus signal
A12	addr[21]		8	O	Address bus signal
B12	addr[22]		8	O	Address bus signal
C12	addr[23]		8	O	Address bus signal
D12	addr[24]		8	O	Address bus signal
A11	addr[25]		8	O	Address bus signal
B11	addr[26]		8	O	Address bus signal
C11	addr[27]		8	O	Address bus signal
G2	clk_en[0]		8	O	SDRAM clock enable
H3	clk_en[1]		8	O	SDRAM clock enable
G1	clk_en[2]		8	O	SDRAM clock enable
H2	clk_en[3]		8	O	SDRAM clock enable
A10	clk_out[0]		8	O	SDRAM clock
A9	clk_out[1]		8	O	SDRAM clock
A5	clk_out[2]		8	O	SDRAM clock
A4	clk_out[3]		8	O	SDRAM clock
G26	data[0]		8	I/O	Data bus signal
H24	data[1]		8	I/O	Data bus signal
G25	data[2]		8	I/O	Data bus signal
F26	data[3]		8	I/O	Data bus signal
G24	data[4]		8	I/O	Data bus signal
F25	data[5]		8	I/O	Data bus signal
E26	data[6]		8	I/O	Data bus signal
F24	data[7]		8	I/O	Data bus signal

Table 4: System Memory interface pinout

Pin #	Signal Name	U/D	OD (mA)	I/O	Description
E25	data[8]		8	I/O	Data bus signal
D26	data[9]		8	I/O	Data bus signal
F23	data[10]		8	I/O	Data bus signal
E24	data[11]		8	I/O	Data bus signal
D25	data[12]		8	I/O	Data bus signal
C26	data[13]		8	I/O	Data bus signal
E23	data[14]		8	I/O	Data bus signal
D24	data[15]		8	I/O	Data bus signal
C25	data[16]		8	I/O	Data bus signal
B26	data[17]		8	I/O	Data bus signal
D22	data[18]		8	I/O	Data bus signal
C23	data[19]		8	I/O	Data bus signal
B24	data[20]		8	I/O	Data bus signal
A25	data[21]		8	I/O	Data bus signal
C22	data[22]		8	I/O	Data bus signal
D21	data[23]		8	I/O	Data bus signal
B23	data[24]		8	I/O	Data bus signal
A24	data[25]		8	I/O	Data bus signal
A23	data[26]		8	I/O	Data bus signal
B22	data[27]		8	I/O	Data bus signal
C21	data[28]		8	I/O	Data bus signal
A22	data[29]		8	I/O	Data bus signal
B21	data[30]		8	I/O	Data bus signal
C20	data[31]		8	I/O	Data bus signal
E1	data_mask[0]		8	O	SDRAM data mask signal
F2	data_mask[1]		8	O	SDRAM data mask signal
G3	data_mask[2]		8	O	SDRAM data mask signal
F1	data_mask[3]		8	O	SDRAM data mask signal
C5	clk_in[0]			I	SDRAM feedback clock
D2	clk_in[1]			I	SDRAM feedback clock
E3	clk_in[2]			I	SDRAM feedback clock
E2	clk_in[3]			I	SDRAM feedback clock

Table 4: System Memory interface pinout

Pin #	Signal Name	U/D	OD (mA)	I/O	Description
B4	byte_lane_sel_n[0]		8	O	Static memory byte lane signal
F4	byte_lane_sel_n[1]		8	O	Static memory byte lane signal
D1	byte_lane_sel_n[2]		8	O	Static memory byte lane signal
F3	byte_lane_sel_n[3]		8	O	Static memory byte lane signal
B5	cas_n		8	O	SDRAM column address strobe
A8	dy_cs_n[0]		8	O	SDRAM chip select signal
B8	dy_cs_n[1]		8	O	SDRAM chip select signal
A6	dy_cs_n[2]		8	O	SDRAM chip select signal
C7	dy_cs_n[3]		8	O	SDRAM chip select signal
C6	st_oe_n		8	O	Static memory output enable
D6	ras_n		8	O	SDRAM row address strobe
H1	dy_pwr_n		8	O	SyncFlash power down
B10	st_cs_n[0]		8	O	Static memory chip select signal
C10	st_cs_n[1]		8	O	Static memory chip select signal
B9	st_cs_n[2]		8	O	Static memory chip select signal
C9	st_cs_n[3]		8	O	Static memory chip select signal
B6	we_n		8	O	SDRAM write enable
J3	ta_strb	U		I	Slow peripheral transfer acknowledge

Table 4: System Memory interface pinout

System Memory interface signals

Table 5 describes the System Memory interface signals in more detail. All signals are internal to the chip.

Name	I/O	Description
addr[27:0]	O	Address output. Used for both static and SDRAM devices. SDRAM memories use bits [14:0]; static memories use bits [25:0].
clk_en[3:0]	O	SDRAM clock enable. Used for SDRAM devices.
clk_out[3:0]	O	SDRAM clocks. Used for SDRAM devices.
data[31:0]	I/O	Read data from memory. Used for the static memory controller, the dynamic memory controller, and the TIC.
data_mask[3:0]	O	Data mask output to SDRAMs. Used for SDRAM devices and static memories.

Table 5: System Memory interface signal descriptions

Name	I/O	Description
clk_in[3:0]	I	Feedback clocks. Used for SDRAM devices.
byte_lane_sel_n[3:0]	O	Byte lane select, active low, for static memories. Used for static memory devices.
cas_n	O	Column address strobe. Used for SDRAM devices.
dy_cs_n[3:0]	O	SDRAM chip selects. Used for SDRAM devices.
st_oe_n	O	Output enable for static memories. Used for static memory devices.
ras_n	O	Row address strobe. Used for SDRAM devices.
st_cs_n[3:0]	O	Static memory chip selects. Default active low. Used for static memory devices.
we_n	O	Write enable. Used for SDRAM and static memories. This signal is used as a test acknowledge during TIC test mode. The test bus acknowledge signal gives external indication that the test bus has been granted and also indicates when a test access has completed. When test acknowledge is low, the current test vector must be extended until test acknowledge becomes high.

Table 5: System Memory interface signal descriptions

Ethernet interface

Pin #	Signal name		U/D	OD (mA)	I/O	Description	
	MII	RMII				MII	RMII
AB1	col	N/C			I	Collision	Pull low external to NS9750
AA2	crs	crs_dv			I	Carrier sense	Carrier sense
AC1	enet_phy_int_n	enet_phy_int_n	U		I	Ethernet PHY interrupt	Ethernet PHY interrupt
AA3	mdc	mdc		4	O	MII management interface clock	MII management interface clock
AB2	mdio	mdio	U	2	I/O	MII management data	MII management data
T3	rx_clk	ref_clk			I	Receive clock	Receive clock
V2	rx_dv	N/C			I	Receive data valid	Pull low external to NS9750
W1	rx_er	rx_er			I	Receive error	Optional signal. Pull low to NS9750 if not used.
V1	rxd[0]	rxd[0]			I	Receive data bit 0	Receive data bit 0
U3	rxd[1]	rxd[1]			I	Receive data bit 1	Receive data bit 1

Table 6: Ethernet interface pinout

Pin #	Signal name		U/D	OD (mA)	I/O	Description	
	MII	RMII				MII	RMII
U2	rxd[2]	N/C			I	Receive data bit 2	Pull low external to NS9750
U1	rxd[3]	N/C			I	Receive data bit 3	Pull low external to NS9750
V3	tx_clk	N/C			I	Transmit clock	Pull low external to NS9750
AA1	tx_en	tx_en		2	O	Transmit enable	Transmit enable
Y3	tx_er	N/C		2	O	Transmit error	N/A
Y2	txd[0]	txd[0]		2	O	Transmit data bit 0	Transmit data bit 0
W3	txd[1]	txd[1]		2	O	Transmit data bit 1	Transmit data bit 1
Y1	txd[2]	N/C		2	O	Transmit data bit 2	Pull low external to NS9750
W2	txd[3]	N/C		2	O	Transmit data bit 3	Pull low external to NS9750

Table 6: Ethernet interface pinout

Clock generation/system pins

Pin #	Signal name	U/D	OD (mA)	I/O	Description
C8	x1_sys_osc			I	System clock crystal oscillator circuit input
B7	x2_sys_osc			O	System clock crystal oscillator circuit output
D9	x1_usb_osc			I	USB clock crystal oscillator circuit input
A7	x2_usb_osc			O	USB clock crystal oscillator circuit output
AC21	reset_done	U	2	I/O	CPU is enabled once the boot program is loaded. Reset_done is set to 1.
H25	reset_n	U		I	System reset input signal
AD20	bist_en_n			I	Enable internal BIST operation
AF21	pll_test_n			I	Enable PLL testing
AE21	scan_en_n			I	Enable internal scan testing
B18	sys_pll_dvdd				System clock PLL 1.5V digital power
A18	sys_pll_dvss				System clock PLL digital ground
B17	sys_pll_avdd				System clock PLL 3.3V analog power

Table 7: Clock generation/system pins pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Description
C17	sys_pll_avss				System clock PLL analog ground
J2	lcdclk	U		I	External LCD clock input
T2	boot_strap[0]	U	2	I/O	Chip select 1 byte lane enable polarity bootstrap select
N3	boot_strap[1]]	U	2	I/O	CardBus mode bootstrap select
P1	boot_strap[2]	U	2	I/O	Memory interface read mode bootstrap select
P2	boot_strap[3]	U	2	I/O	Chip select 1 data width bootstrap select
P3	boot_strap[4]	U	2	I/O	Chip select 1 data width bootstrap select

Table 7: Clock generation/system pins pinout

PCI interface

The PCI interface can be set to PCI host or PCI device (slave) using the `boot_strap[1]` pin (see "System configuration" on page 5). If not using the PCI interface, all inputs must be pulled up, with the exception of `AD[31:0]`, `C/BE[3:0]`, and `PAR`.

Note: All output drivers for PCI meet the standard PCI driver specification.

Pin #	Signal Name	U/D	OD (mA)	I/O	Description
J24	ad[0]		N/A	I/O	PCI time-multiplexed address/data bus
H26	ad[1]		N/A	I/O	PCI time-multiplexed address/data bus
J25	ad[2]		N/A	I/O	PCI time-multiplexed address/data bus
J26	ad[3]		N/A	I/O	PCI time-multiplexed address/data bus
K24	ad[4]		N/A	I/O	PCI time-multiplexed address/data bus
K25	ad[5]		N/A	I/O	PCI time-multiplexed address/data bus
K26	ad[6]		N/A	I/O	PCI time-multiplexed address/data bus
L24	ad[7]		N/A	I/O	PCI time-multiplexed address/data bus
L26	ad[8]		N/A	I/O	PCI time-multiplexed address/data bus
M24	ad[9]		N/A	I/O	PCI time-multiplexed address/data bus
M25	ad[10]		N/A	I/O	PCI time-multiplexed address/data bus
M26	ad[11]		N/A	I/O	PCI time-multiplexed address/data bus
N24	ad[12]		N/A	I/O	PCI time-multiplexed address/data bus
N25	ad[13]		N/A	I/O	PCI time-multiplexed address/data bus
N26	ad[14]		N/A	I/O	PCI time-multiplexed address/data bus

Table 8: PCI interface pinout

Pin #	Signal Name	U/D	OD (mA)	I/O	Description
P26	ad[15]		N/A	I/O	PCI time-multiplexed address/data bus
U24	ad[16]		N/A	I/O	PCI time-multiplexed address/data bus
V26	ad[17]		N/A	I/O	PCI time-multiplexed address/data bus
V25	ad[18]		N/A	I/O	PCI time-multiplexed address/data bus
W26	ad[19]		N/A	I/O	PCI time-multiplexed address/data bus
V24	ad[20]		N/A	I/O	PCI time-multiplexed address/data bus
W25	ad[21]		N/A	I/O	PCI time-multiplexed address/data bus
Y26	ad[22]		N/A	I/O	PCI time-multiplexed address/data bus
W24	ad[23]		N/A	I/O	PCI time-multiplexed address/data bus
Y24	ad[24]		N/A	I/O	PCI time-multiplexed address/data bus
AA25	ad[25]		N/A	I/O	PCI time-multiplexed address/data bus
AB26	ad[26]		N/A	I/O	PCI time-multiplexed address/data bus
AA24	ad[27]		N/A	I/O	PCI time-multiplexed address/data bus
AB25	ad[28]		N/A	I/O	PCI time-multiplexed address/data bus
AC26	ad[29]		N/A	I/O	PCI time-multiplexed address/data bus
AD26	ad[30]		N/A	I/O	PCI time-multiplexed address/data bus
AC25	ad[31]		N/A	I/O	PCI time-multiplexed address/data bus
L25	cbe_n[0]		N/A	I/O	Command/byte enable
P25	cbe_n[1]		N/A	I/O	Command/byte enable
U25	cbe_n[2]		N/A	I/O	Command/byte enable
AA26	cbe_n[3]		N/A	I/O	Command/byte enable
T26	devsel_n		N/A	I/O	Device select
U26	frame_n		N/A	I/O	Cycle frame
Y25	idsel		N/A	I	Initialization device select
T24	irdy_n		N/A	I/O	Initiator ready
P24	par		N/A	I/O	Parity signal
R25	perr_n		N/A	I/O	Parity error
R26	serr_n		N/A	I/O	System error: Input: `pci_central_resource_n` = 0 Output: `pci_central_resource_n` = 1
R24	stop_n		N/A	I/O	Stop signal
T25	trdy_n		N/A	I/O	Target ready

Table 8: PCI interface pinout

Pin #	Signal Name	U/D	OD (mA)	I/O	Description
AC24	pci_arb_gnt_1_n		N/A	O	PCI channel 1 grant
AD23	pci_arb_gnt_2_n		N/A	O	PCI channel 2 grant
AE24	pci_arb_gnt_3_n		N/A	O	PCI channel 3 grant
AD25	pci_arb_req_1_n		N/A	I	PCI channel 1 request
AB23	pci_arb_req_2_n		N/A	I	PCI channel 2 request
AC22	pci_arb_req_3_n		N/A	I	PCI channel 3 request
AF23	pci_central_resource_n	D	N/A	I	PCI internal central resource enable
AF25	pci_int_a_n		N/A	I/O	PCI interrupt request A, output if external central resource used
AF24	pci_int_b_n		N/A	I/O	PCI interrupt request B, CCLKRUN# for CardBus applications
AE23	pci_int_c_n		N/A	I	PCI interrupt request C
AD22	pci_int_d_n		N/A	I	PCI interrupt request D
AE26	pci_reset_n		N/A	I/O	PCI reset, output if internal central resource enabled
AB24	pci_clk_in	U	N/A	I	PCI clock in
AA23	pci_clk_out		N/A	O	PCI clock out

Table 8: PCI interface pinout

PCI/CardBus signals

Most of the CardBus signals are the same as the PCI signals. Other CardBus signals are unique and multiplexed with PCI signals for NS9750. Table 9 shows these signals.

PCI signal	CardBus signal	CardBus type	Description
INTA#	CINT#	Input	CardBus interrupt pin. The `INTA2PCI` pin in the PCI Miscellaneous Support register must be set to 0.
INTB#	CCLKRUN#	Bidir	CardBus pin used to negotiate with the external CardBus device before stopping the clock. Allows external CardBus device to request that the clock be restarted.
INTC#	CSTSCHG	Input	CardBus status change interrupt signal.
GNT1#	CGNT#	Output	Grant to external CardBus device from NS9750's internal arbiter.

Table 9: CardBus IO muxed signals

PCI signal	CardBus signal	CardBus type	Description
GNT2#	CVS1	Output	Voltage sense pin. Normally driven low by NS9750, but toggled during interrogation of the external CardBus device to find voltage requirements.
GNT3#	CVS2	Output	Voltage sense pin. Normally driven low by NS9750, but toggled during interrogation of the external CardBus device to find voltage requirements.
REQ1#	CREQ#	Input	Request from external CardBus device to NS9750's internal arbiter.
REQ2#	CCD1	Input	Card detect pin. Pulled up when the socket is empty and pulled low when the external CardBus device is in the socket.
REQ3#	CCD2	Input	Card detect pin. Pulled up when the socket is empty and pulled low when the external CardBus device is in the socket.

Table 9: CardBus IO muxed signals

GPIO MUX

Note: The BBus utility contains the control pins for each GPIO MUX bit. Each pin can be selected individually; that is, you can select any option (00, 01, 02, 03) for any pin, by setting the appropriate bit in the appropriate register. Some signals are muxed to two different GPIO pins, to maximize the number of possible applications. These duplicate signals are marked as such in the Descriptions column in the table.

The 00 option for the serial ports (A, B, C, and D) are configured for UART, HDLC, and SPI mode, respectively; that is the UART option is shown first, followed by the HDLC option if there is one, followed by the SPI option if there is one. If only one value appears, it is the UART mode value. SPI options all begin with *SPI*. HDLC includes an external driver enable function, DEN; you can use any available GPIO MUX pin (depending on your configuration) for this function.

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)
AF19	gpio[0]	U	2	I/O	00 Ser port A TxData / Ser port A TxData / SPI port A dout 01 DMA ch 0 done (duplicate) 02 Timer 1 (duplicate) 03 GPIO 0

Table 10: GPIO MUX pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)	
AE18	gpio[1]	U	2	I/O	00	Ser port A RxData / Ser port A RxData / SPI port A din
					01	DMA ch 0 req (duplicate)
					02	Ext IRQ 0
					03	GPIO 1
AF18	gpio[2]	U	2	I/O	00	Ser port A RTS
					01	Timer 0
					02	DMA ch 1 ack
					03	GPIO 2
AD17	gpio[3]	U	2	I/O	00	Ser port A CTS
					01	1284 nAck (peripheral-driven)
					02	DMA ch 0 req
					03	GPIO 3
AE17	gpio[4]	U	2	I/O	00	Ser port A DTR
					01	1284 busy (peripheral-driven)
					02	DMA ch 0 done
					03	GPIO 4
AF17	gpio[5]	U	2	I/O	00	Ser port A DSR
					01	1284 PError (peripheral-driven)
					02	DMA ch 0 ack
					03	GPIO 5
AD16	gpio[6]	U	2	I/O	00	Ser port A RI / Ser port A RxClk / SPI port A clk
					01	1284 nFault (peripheral-driven)
					02	Timer 7 (duplicate)
					03	GPIO 6
AE16	gpio[7]	U	2	I/O	00	Ser port A DCD / Ser port A TxClk / SPI port A enable
					01	DMA ch 0 ack (duplicate)
					02	Ext IRQ 1
					03	GPIO 7
AD15	gpio[8]	U	2	I/O	00	Ser port B TxData / Ser port B TxData / SPI port B dout
					01	Reserved
					02	Reserved
					03	GPIO 8
AE15	gpio[9]	U	2	I/O	00	Ser port B RxData / Ser port B RxData / SPI port B din
					01	Reserved
					02	Timer 8 (duplicate)
					03	GPIO 9

Table 10: GPIO MUX pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)
AF15	gpio[10]	U	2	I/O	00 Ser port B RTS 01 Reserved 02 Reserved 03: GPIO 10
AD14	gpio[11]	U	2	I/O	00 Ser port B CTS 01 IRQ2 (duplicate) 02 Timer 0 (duplicate) 03 GPIO 11
AE14	gpio[12]	U	2	I/O	00 Ser port B DTR 01 Reserved 02 Reserved 03 GPIO 12
AF14	gpio[13]	U	2	I/O	00 Ser port B DSR 01 Ext IRQ 0 (duplicate) 02 Timer 10 (duplicate) 03 GPIO 13
AF13	gpio[14]	U	2	I/O	00 Ser port B RI / Ser port B RxClk / SPI port B clk 01 Timer 1 02 Reserved 03 GPIO 14
AE13	gpio[15]	U	2	I/O	00 Ser port B DCD / Ser port B TxClk / Ser port B enable 01 Timer 2 02 Reserved 03 GPIO 15
AD13	gpio[16]	U	2	I/O	00 USB overcurrent 01 1284 nFault (peripheral-driven, duplicate) 02 Timer 11 (duplicate) 03 GPIO 16
AF12	gpio[17]	U	2	I/O	00 USB power relay 01 Reserved 02 Reserved 03 GPIO 17
AE12	gpio[18]	U	4	I/O	00 Ethernet CAM reject 01 LCD power enable 02 Ext IRQ 3 (duplicate) 03 GPIO 18

Table 10: GPIO MUX pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)
AD12	gpio[19]	U	4	I/O	00 Ethernet CAM req 01 LCD line-horz sync 02 DMA ch 1 ack 03 GPIO 19
AC12	gpio[20]	U	8	I/O	00 Ser port C DTR 01 LCD clock 02 Reserved 03 GPIO 20
AF11	gpio[21]	U	4	I/O	00 Ser port C DSR 01 LCD frame pulse-vert 02 Reserved 03 GPIO 21
AE11	gpio[22]	U	4	I/O	00 Ser port C RI / Ser port C RxClk / SPI port C clk 01 LCD AC bias-data enable 02 Reserved 03 GPIO 22
AD11	gpio[23]	U	4	I/O	00 Ser port C DCD / Ser port C TxClk / SPI port C enable 01 LCD line end 02 Timer 14 (duplicate) 03 GPIO 23
AF10	gpio[24]	U	4	I/O	00 Ser port D DTR 01 LCD data bit 0 02 Reserved 03 GPIO 24
AE10	gpio[25]	U	4	I/O	00 Ser port D DSR 01 LCD data bit 1 02 Timer 15 (duplicate) 03 GPIO 25
AD10	gpio[26]	U	4	I/O	00 Ser port D RI / Ser port D RxClk / SPI port D clk 01 LCD data bit 2 02 Timer 3 03 GPIO 26
AF9	gpio[27]	U	4	I/O	00 Ser port D DCD / Ser port D TxClk / SPI port D enable 01 LCD data bit 3 02 Timer 4 03 GPIO 27

Table 10: GPIO MUX pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)	
AE9	gpio[28]	U	4	I/O	00	Ext IRQ 1 (duplicate)
					01	LCD data bit 4
					02	LCD data bit 8 (duplicate)
					03	GPIO 28
AF8	gpio[29]	U	4	I/O	00	Timer 5
					01	LCD data bit 5
					02	LCD data bit 9 (duplicate)
					03	GPIO 29
AD9	gpio[30]	U	4	I/O	00	Timer 6
					01	LCD data bit 6
					02	LCD data bit 10 (duplicate)
					03	GPIO 30
AE8	gpio[31]	U	4	I/O	00	Timer 7
					01	LCD data bit 7
					02	LCD data bit 11 (duplicate)
					03	GPIO 31
AF7	gpio[32]	U	4	I/O	00	Ext IRQ 2
					01	1284 Data 1 (bidirectional)
					02	LCD data bit 8
					03	GPIO 32
AD8	gpio[33]	U	4	I/O	00	Timer 8
					01	1284 Data 2 (bidirectional)
					02	LCD data bit 9
					03	GPIO 33
AD7	gpio[34]	U	4	I/O	00	Timer 9
					01	1284 Data 3 (bidirectional)
					02	LCD data bit 10
					03	GPIO 34
AE6	gpio[35]	U	4	I/O	00	Timer 10
					01	1284 Data 4 (bidirectional)
					02	LCD data bit 11
					03	GPIO 35
AF5	gpio[36]	U	4	I/O	00	Reserved
					01	1284 Data 5 (bidirectional)
					02	LCD data bit 12
					03	GPIO 36
AD6	gpio[37]	U	4	I/O	00	Reserved
					01	1284 Data 6 (bidirectional)
					02	LCD data bit 13
					03	GPIO 37

Table 10: GPIO MUX pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)
AE5	gpio[38]	U	4	I/O	00 Reserved 01 1284 Data 7 (bidirectional) 02 LCD data bit 14 03 GPIO 38
AF4	gpio[39]	U	4	I/O	00 Reserved 01 1284 Data 8 (bidirectional) 02 LCD data bit 15 03 GPIO 39
AC6	gpio[40]	U	4	I/O	00 Ser port C TxData / Ser port C TxData / SPI port C dout 01 Ext IRQ 3 02 LCD data bit 16 03 GPIO 40
AD5	gpio[41]	U	4	I/O	00 Ser port C RxData / Ser port C RxData / SPI port C din 01 Timer 11 02 LCD data bit 17 03 GPIO 41
AE4	gpio[42]	U	4	I/O	00 Ser port C RTS 01 Timer 12 02 LCD data bit 18 03 GPIO 42
AF3	gpio[43]	U	4	I/O	00 Ser port C CTS 01 Timer 13 02 LCD data bit 19 03 GPIO 43
AD2	gpio[44]	U	4	I/O	00 Ser port D TxData / Ser port D TxData / SPI port D dout 01 1284 Select (peripheral-driven) 02 LCD data bit 20 03 GPIO 44
AE1	gpio[45]	U	4	I/O	00 Ser port D RxData / Ser port D RxData / SPI port D din 01 1284 nStrobe (host-driven) 02 LCD data bit 21 03 GPIO 45
AB3	gpio[46]	U	4	I/O	00 Ser port D RTS 01 1284 nAutoFd (host-driven) 02 LCD data bit 22 03 GPIO 46

Table 10: GPIO MUX pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)
AA4	gpio[47]	U	4	I/O	00 Ser port D CTS 01 1284 nInit (host-driven) 02 LCD data bit 23 03 GPIO 47
AC2	gpio[48]	U	2	I/O	00 Timer 14 01 1284 SelectIn (host-driven) 02 DMA ch 1 req 03 GPIO 48
AD1	gpio[49]	U	2	I/O	00 Timer 15 01 1284 Peripheral Logic High (peripheral-driven) 02 DMA ch 1 done 03 GPIO 49

Table 10: GPIO MUX pinout

LCD module signals

The LCD module signals are multiplexed with GPIO pins. They include six control signals and up to 24 data signals. Table 11 describes the control signals. Table 12 and Table 13 provide details for the data signals.

Signal name	Type	Description
CLPOWER	Output	LCD panel power enable
CLLP	Output	Line synchronization pulse (STN) / horizontal synchronization pulse (TFT)
CLCP	Output	LCD panel clock
CLFP	Output	Frame pulse (STN) / vertical synchronization pulse (TFT)
CLAC	Output	STN AC bias drive or TFT data enable output
CLD[23:0]	Output	LCD panel data (see Table 12 and Table 13)
CLLE	Output	Line end signal

Table 11: LCD module signal descriptions

The `CLD[23:0]` signal has eight modes of operation:

- TFT 24-bit interface
- TFT 18-bit interface
- Color STN single panel
- Color STN dual panel
- 4-bit mono STN single panel
- 4-bit mono STN dual panel
- 8-bit mono STN single panel
- 8-bit mono STN dual panel

Table 12 shows which CLD[23:0] pins provide the pixel data to the STN panel for each mode of operation.

Legend:

- Ext pin = External pin
- CUSTN = Color upper panel STN, dual and/or single panel
- CLSTN = Color lower panel STN, single
- MUSTN = Mono upper panel STN, dual and/or single panel
- MLSTN = Mono lower panel STN, single
- N/A = not used
- 01 and 02 = The option number/position in the Description field of the GPIO mux pinout. See "GPIO MUX" on page 21 for more information.

Ext pin	GPIO pin & description	Color STN single panel	Color STN dual panel	4-bit mono STN single panel	4-bit mono STN dual panel	8-bit mono STN single panel	8-bit mono STN dual panel
CLD[23]	AB1 = LCD data bit 23 (02)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[22]	AA3 = LCD data bit 22 (02)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[21]	AB2 = LCD data bit 21 (02)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[20]	AC1 = LCD data bit 20 (02)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[19]	AA4 = LCD data bit 19 (02)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[18]	AF2 = LCD data bit 18 (02)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[17]	AD4 = LCD data bit 17 (02)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[16]	AF3 = LCD data bit16 (02)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[15]	AE4 = LCD data bit 15 (02)	N/A	CLSTN[0][1]	N/A	N/A	N/A	MLSTN[0][1]
CLD[14]	AF4 = LCD data bit 14 (02)	N/A	CLSTN[1]	N/A	N/A	N/A	MLSTN[1]
CLD[13]	AE5 = LCD data bit 13 (02)	N/A	CLSTN[2]	N/A	N/A	N/A	MLSTN[2]
CLD[12]	AD6 = LCD data bit 12 (02)	N/A	CLSTN[3]	N/A	N/A	N/A	MLSTN[3]
CLD[11]	AF7 = LCD data bit 11 (02) AF5 = LCD data bit 11 (02)	N/A	CLSTN[4]	N/A	MLSTN[0][1]	N/A	MLSTN[4]
CLD[10]	AE8 = LCD data bit 10 (02) AE6 = LCD data bit 10 (02)	N/A	CLSTN[5]	N/A	MLSTN[1]	N/A	MLSTN[5]
CLD[9]	AF8 = LCD data bit 9 (02) AE7 = LCD data bit 9 (02)	N/A	CLSTN[6]	N/A	MLSTN[2]	N/A	MLSTN[6]
CLD[8]	AD9 = LCD data bit 8 (02) AD8 = LCD data bit 8 (02)	N/A	CLSTN[7]	N/A	MLSTN[3]	N/A	MLSTN[7]
CLD[7]	AF7 = LCD data bit 7 (01)	CUSTN[0][1]	CUSTN[0][1]	N/A	N/A	MUSTN[0]	MUSTN[0][1]

Table 12: CLD[23:0] pin descriptions for STN display

Ext pin	GPIO pin & description	Color STN single panel	Color STN dual panel	4-bit mono STN single panel	4-bit mono STN dual panel	8-bit mono STN single panel	8-bit mono STN dual panel
CLD[6]	AE8 = LCD data bit 6 (01)	CUSTN[1]	CUSTN[1]	N/A	N/A	MUSTN[1]	MUSTN[1]
CLD[5]	AF8 = LCD data bit 5 (01)	CUSTN[2]	CUSTN[2]	N/A	N/A	MUSTN[2]	MUSTN[2]
CLD[4]	AD9 = LCD data bit 4 (01)	CUSTN[3]	CUSTN[3]	N/A	N/A	MUSTN[3]	MUSTN[3]
CLD[3]	AE9 = LCD data bit 3 (01)	CUSTN[4]	CUSTN[4]	MUSTN[0]	MUSTN[0][1]	MUSTN[4]	MUSTN[4]
CLD[2]	AC9 = LCD data bit 2 (01)	CUSTN[5]	CUSTN[5]	MUSTN[1]	MUSTN[1]	MUSTN[5]	MUSTN[5]
CLD[1]	AF9 = LCD data bit 1(01)	CUSTN[6]	CUSTN[6]	MUSTN[2]	MUSTN[2]	MUSTN[6]	MUSTN[6]
CLD[0]	AE10 = LCD data bit 0 (01)	CUSTN[7]	CUSTN[7]	MUSTN[3]	MUSTN[3]	MUSTN[7]	MUSTN[7]

1 This data bit corresponds to the first "pixel position." For example, for an 8-bit mono STN display, `CUSTN[0]` is the leftmost pixel on the panel and `CUSTN[7]` is the rightmost pixel within the 8-bit data. For a color STN display, bits [7, 6, 5] form the leftmost pixel.

Table 12: CLD[23:0] pin descriptions for STN display

Table 13 shows which `CLD[23:0]` pins provide the pixel data to the TFT panel for each of the multiplexing modes of operation.

External pin	TFT 24 bit	TFT 18 bit
CLD[23]	BLUE[7]	Reserved
CLD[22]	BLUE[6]	Reserved
CLD[21]	BLUE[5]	Reserved
CLD[20]	BLUE[4]	Reserved
CLD[19]	BLUE[3]	Reserved
CLD[18]	BLUE[2]	Reserved
CLD[17]	BLUE[1]	BLUE[4]
CLD[16]	BLUE[0]	BLUE[3]
CLD[15]	GREEN[7]	BLUE[2]
CLD[14]	GREEN[6]	BLUE[1]
CLD[13]	GREEN[5]	BLUE[0]
CLD[12]	GREEN[4]	Intensity bit
CLD[11]	GREEN[3]	GREEN[4]
CLD[10]	GREEN[2]	GREEN[3]
CLD[9]	GREEN[1]	GREEN[2]

Table 13: CLD[23:0] pin descriptions for TFT display

External pin	TFT 24 bit	TFT 18 bit
CLD[8]	GREEN[0]	GREEN[1]
CLD[7]	RED[7]	GREEN[0]
CLD[6]	RED[6]	Intensity bit
CLD[5]	RED[5]	RED[4]
CLD[4]	RED[4]	RED[3]
CLD[3]	RED[3]	RED[2]
CLD[2]	RED[2]	RED[1]
CLD[1]	RED[1]	RED[0]
CLD[0]	RED[0]	Intensity bit

Table 13: CLD[23:0] pin descriptions for TFT display

I²C interface

Pin #	Signal name	U/D	OD (mA)	I/O	Description
AC15	iic_scl		4	I/O	I²C serial clock line
AF16	iic_sda		4	I/O	I²C serial data line

Table 14: I²C interface pinout

USB Interface

Notes:

- If not using the USB interface, these pins should be pulled down to ground through a 15K ohm resistor.
- All output drivers for USB meet the standard USB driver specification.

Pin #	Signal name	U/D	OD (mA)	I/O	Description
AB4	usb_dm			I/O	USB data -
AC3	usb_dp			I/O	USB data +

Table 15: USB interface pinout

JTAG interface for ARM core/boundary scan

Note: `trst_n` must be pulsed low to initialize the JTAG when a debugger is not attached.

Pin #	Signal name	U/D	OD (mA)	I/O	Description
AE20	tck			I	Test clock
AD18	tdi	U		I	Test data in
AE19	tdo		2	O	Test data out
AC18	tms	U		I	Test mode select
AF20	trst_n	U		I	Test mode reset
AD19	rtck	U	2	I/O	Returned test clock, ARM core only

Table 16: JTAG interface/boundary scan pinout

Reserved pins

Pin#	Description
J1	Tie to ground directly
K3	Tie to ground directly
K2	Tie to ground directly
K1	Tie to ground directly
R1	Tie to ground directly
R2	Tie to ground directly
R3	Tie to ground directly
T1	Tie to ground directly
AF6	Tie to ground directly
AE3	Tie to ground directly
AC5	Tie to ground directly
AD4	Tie to 1.5V core power
AF2	Tie to 3.3V I/O power
AE7	No connect
L3	No connect
L2	No connect
L1	No connect
M3	No connect

Table 17: Reserved pins

Pin#	Description
M2	Tie to ground directly
M1	Tie to ground directly
N1	Tie to ground directly
N2	Tie to ground directly
AF22	No connect
AD21	No connect
AE22	No connect

Table 17: Reserved pins

Power ground

Pin #	Signal name	Description
J23, L23, K23, U23, T23, V23, D18, D17, AC17, D16, AC16, D11, D10, AC11, AC10, AC9, J4, L4, K4, U4, T4, V4	VDDC	Core power, 1.5V
G23, H23, M23, R23, P23, N23, Y23, W23, D20, AC20, D19, AC19, D14, D13, AC14, AC13, D8, D7, AC8, AC7, G4, H4, M4, R4, P4, N4, Y4, W4	VDDS	I/O power, 3.3V
A26, B25, AE25, AF26, D23, C24, AD24, AC23, D5, D4, C4, E4, AC4, A3, A2, D3, C3, C2, B3, B2, AE2, AD3, A1, C1, B1, AF1	VSS2	Ground

Table 18: Power ground pins

Address and register maps

System address map

The system memory address is divided to allow access to the internal and external resources on the system bus, as shown in Table 19.

Address range	Size	System functions
0x0000 0000 – 0x0FFF FFFF	256 MB	System memory chip select 4 - Dynamic memory (default)
0x1000 0000 – 0x1FFF FFFF	256 MB	System memory chip select 5 - Dynamic memory (default)
0x2000 0000 – 0x2FFF FFFF	256 MB	System memory chip select 6 - Dynamic memory (default)
0x3000 0000 – 0x3FFF FFFF	256 MB	System memory chip select 7 - Dynamic memory (default)
0x4000 0000 – 0x4FFF FFFF	256 MB	System memory chip select 0 - Static memory (default)
0x5000 0000 – 0x5FFF FFFF	256 MB	System memory chip select 1 - Static memory (default)
0x6000 0000 – 0x6FFF FFFF	256MB	System memory chip select 2 - Static memory (default)
0x7000 0000 – 0x7FFF FFFF	256 MB	System memory chip select 3 - Static memory (default)
0x8000 0000 – 0x8FFF FFFF	256 MB	PCI memory
0x9000 0000 – 0x9FFF FFFF	256 MB	BBus memory
0xA000 0000 – 0xA00F FFFF	1 MB	PCI IO
0xA010 0000 – 0xA01F FFFF	1 MB	PCI CONFIG_ADDR
0xA020 0000 – 0xA02F FFFF	1 MB	PCI CONFIG_DATA
0xA030 0000 – 0xA03F FFFF	1 MB	PCI arbiter
0xA040 0000 – 0xA04F FFFF	1 MB	BBus-to-AHB bridge
0xA050 0000 – 0xA05F FFFF	1 MB	Reserved
0xA060 0000 – 0xA06F FFFF	1 MB	Ethernet Communication module
0xA070 0000 – 0xA07F FFFF	1 MB	Memory controller
0xA080 0000 – 0xA08F FFFF	1 MB	LCD controller
0xA090 0000 – 0xA09F FFFF	1 MB	System Control module
0xA0A0 0000 – 0xFFFF FFFF	1526 MB	Reserved

Table 19: System address memory map

BBus peripheral address map

The BBus bridge configuration registers are located at base address 0xA040 0000. The BBus peripherals are located at base address 0x9000 0000 and span a 256 MB address space. Each BBus peripheral, with the exception of the SER controllers, resides in a 1 MB address space. Table 20 specifies the address space given to each peripheral.

Base address	Peripheral
0x9000 0000	BBus DMA controller
0x9010 0000	USB controller
0x9020 0000	SER Port #1
0x9020 0040	SER Port #2
0x9030 0000	SER Port #3
0x9030 0040	SER Port #4
0x9040 0000	IEEE 1284 controller
0x9050 0000	I^2C controller
0x9060 0000	BBus utility

Table 20: BBus peripheral address map

System Control registers

Address	31:24	23:16	15:08	07:00
A090 0000	AHB Arbiter Gen Configuration			
A090 0004	BRC0			
A090 0008	BRC1			
A090 000C	BRC2			
A090 0010	BRC3			
A090 0014	AHB Bus Arbiter Timeout Period		AHB Bus Monitor Timeout Period	
A090 0018	AHB Error Detect Status 1			
A090 001C	AHB Error Detect Status 2			
A090 0020	AHB Error Monitoring Configuration			
A090 0024	Reserved			
A090 0028	Reserved			
A090 002C	Reserved			
A090 0030	Reserved			
A090 0034	Reserved			
A090 0038	Reserved			
A0090 003C	Reserved			
A090 0040	Reserved			
A090 0044	Timer 0 Reload Count register			

Table 21: System Control register map

Address	31:24	23:16	15:08	07:00
A090 0048	Timer 1 Reload Count register			
A090 004C	Timer 2 Reload Count register			
A090 0050	Timer 3 Reload Count register			
A090 0054	Timer 4 Reload Count register			
A090 0058	Timer 5 Reload Count register			
A090 005C	Timer 6 Reload Count register			
A090 0060	Timer 7 Reload Count register			
A090 0064	Timer 8 Reload Count register			
A090 0068	Timer 9 Reload Count register			
A090 006C	Timer 10 Reload Count register			
A090 0070	Timer 11 Reload Count register			
A090 0074	Timer 12 Reload Count register			
A090 0078	Timer 13 Reload Count register			
A090 007C	Timer 14 Reload Count register			
A090 0080	Timer 15 Reload Count register			
A090 0084	Timer 0 Read register			
A090 0088	Timer 1 Read register			
A090 008C	Timer 2 Read register			
A090 0090	Timer 3 Read register			
A090 0094	Timer 4 Read register			
A090 0098	Timer 5 Read register			
A090 009C	Timer 6 Read register			
A090 00A0	Timer 7 Read register			
A090 00A4	Timer 8 Read register			
A090 00A8	Timer 9 Read register			
A090 00AC	Timer 10 Read register			
A090 00B0	Timer 11 Read register			
A090 00B4	Timer 12 Read register			
A090 00B8	Timer 13 Read register			
A090 00BC	Timer 14 Read register			
A090 00C0	Timer 15 Read register			
A090 00C4	Interrupt Vector Address Register Level 0			

Table 21: System Control register map

Address	31:24	23:16	15:08	07:00
A090 00C8	Interrupt Vector Address Register Level 1			
A090 00CC	Interrupt Vector Address Register Level 2			
A090 00D0	Interrupt Vector Address Register Level 3			
A090 00D4	Interrupt Vector Address Register Level 4			
A090 00D8	Interrupt Vector Address Register Level 5			
A090 00DC	Interrupt Vector Address Register Level 6			
A090 00E0	Interrupt Vector Address Register Level 7			
A090 00E4	Interrupt Vector Address Register Level 8			
A090 00E8	Interrupt Vector Address Register Level 9			
A090 00EC	Interrupt Vector Address Register Level 10			
A090 00F0	Interrupt Vector Address Register Level 11			
A090 00F4	Interrupt Vector Address Register Level 12			
A090 00F8	Interrupt Vector Address Register Level 13			
A090 00FC	Interrupt Vector Address Register Level 14			
A090 0100	Interrupt Vector Address Register Level 15			
A090 0104	Interrupt Vector Address Register Level 16			
A090 0108	Interrupt Vector Address Register Level 17			
A090 010C	Interrupt Vector Address Register Level 18			
A090 0110	Interrupt Vector Address Register Level 19			
A090 0114	Interrupt Vector Address Register Level 20			
A090 0118	Interrupt Vector Address Register Level 21			
A090 011C	Interrupt Vector Address Register Level 22			
A090 0120	Interrupt Vector Address Register Level 23			
A090 0124	Interrupt Vector Address Register Level 24			
A090 0128	Interrupt Vector Address Register Level 25			
A090 012C	Interrupt Vector Address Register Level 26			
A090 0130	Interrupt Vector Address Register Level 27			
A090 0134	Interrupt Vector Address Register Level 28			
A090 0138	Interrupt Vector Address Register Level 29			
A090 013C	Interrupt Vector Address Register Level 30			
A090 0140	Interrupt Vector Address Register Level 31			
A090 0144	Int Config 0	Int Config 1	Int Config 2	Int Config 3

Table 21: System Control register map

Address	31:24	23:16	15:08	07:00
A090 0148	Int Config 4	Int Config 5	Int Config 6	Int Config 7
A090 014C	Int Config 8	Int Config 9	Int Config 10	Int Config 11
A090 0150	Int Config 12	Int Config 13	Int Config 14	Int Config 15
A090 0154	Int Config 16	Int Config 17	Int Config 18	Int Config 19
A090 0158	Int Config 20	Int Config 21	Int Config 22	Int Config 23
A090 015C	Int Config 24	Int Config 25	Int Config 26	Int Config 27
A090 0160	Int Config 28	Int Config 29	Int Config 30	Int Config 31
A090 0164	ISRADDR			
A090 0168	Interrupt Status Active			
A090 016C	Interrupt Status Raw			
A090 0170	Timer Interrupt Status register			
A090 0174	Software Watchdog Configuration			
A090 0178	Software Watchdog Timer			
A090 017C	Clock Configuration register			
A090 0180	Module Reset register			
A090 0184	Miscellaneous System Configuration register			
A090 0188	PLL Configuration register			
A090 018C	Active Interrupt ID			
A090 0190	Timer 0 Control register			
A090 0194	Timer 1 Control register			
A090 0198	Timer 2 Control register			
A090 019C	Timer 3 Control register			
A090 01A0	Timer 4 Control register			
A090 01A4	Timer 5 Control register			
A090 01A8	Timer 6 Control register			
A090 01AC	Timer 7 Control register			
A090 01B0	Timer 8 Control register			
A090 01B4	Timer 9 Control register			
A90 01B8	Timer 10 Control register			
A090 01BC	Timer 11 Control register			
A090 01C0	Timer 12 Control register			
A090 01C4	Timer 13 Control register			

Table 21: System Control register map

Address	31:24	23:16	15:08	07:00
A090 01C8	Timer 14 Control register			
A090 01CC	Timer 15 Control register			
A090 01D0	System Memory Chip Select 4 Dynamic Memory Base			
A090 01D4	System Memory Chip Select 4 Dynamic Memory Mask			
A090 01D8	System Memory Chip Select 5 Dynamic Memory Base			
A090 01DC	System Memory Chip Select 5 Dynamic Memory Mask			
A090 01E0	System Memory Chip Select 6 Dynamic Memory Base			
A090 01E4	System Memory Chip Select 6 Dynamic Memory Mask			
A090 01E8	System Memory Chip Select 7 Dynamic Memory Base			
A090 01EC	System Memory Chip Select 7 Dynamic Memory Mask			
A090 01F0	System Memory Chip Select 0 Static Memory Base			
A090 01F4	System Memory Chip Select 0 Static Memory Mask			
A090 01F8	System Memory Chip Select 1 Static Memory Base			
A090 01FC	System Memory Chip Select 1 Static Memory Mask			
A090 0200	System Memory Chip Select 2 Static Memory Base			
A090 0204	System Memory Chip Select 2 Static Memory Mask			
A090 0208	System Memory Chip Select 3 Static Memory Base			
A090 020C	System Memory Chip Select 3 Static Memory Mask			
A090 0210	GenID			

Table 21: System Control register map

Memory Controller registers

Address	Register	Description
A070 0000	MPMCControl	Control register
A070 0004	MPMCStatus	Status register
A070 0008	MPMCConfig	Configuration register
A070 0020	MPMCDynamicControl	Dynamic Memory Control register
A070 0024	MPMCDynamicRefresh	Dynamic Memory Refresh Timer
A070 0030	MPMCDynamictRP	Dynamic Memory Precharge Command Period (t_{RP})
A070 0034	MPMCDynamictRAS	Dynamic Memory Active to Precharge Command Period (t_{RAS})
A070 0038	MPMCDynamictSREX	Dynamic Memory Self-Refresh Exit Time (t_{SREX})

Table 22: Memory Controller register map

Address	Register	Description
A070 003C	MPMCDynamictAPR	Dynamic Memory Last Data Out to Active Time (t_{APR})
A070 0040	MPMCDynamictDAL	Dynamic Memory Data-in to Active Command Time (t_{DAL} or t_{APW})
A070 0044	MPMCDynamictWR	Dynamic Memory Write Recovery Time (t_{WR}, t_{DPL}, t_{RWL}, or t_{RDL})
A070 0048	MPMCDynamictRC	Dynamic Memory Active to Active Command Period (t_{RC})
A070 004C	MPMCDynamictRFC	Dynamic Memory Auto Refresh Period, and Auto Refresh to Active Command Period (t_{RFC})
A070 0050	MPMCDynamictXSR	Dynamic Memory Exit Self-Refresh to Active Command Time (t_{XSR})
A070 0054	MPMCDynamictRRD	Dynamic Memory Active Bank A to Active B Time (t_{RRD})
A070 0058	MPMCDynamictMRD	Dynamic Memory Load Mode Register to Active Command Time (t_{MRD})
A070 0080	MPMCStaticExtendedWait	Static Memory Extended Wait
A070 0100	MPMCDynamicConfig0	Dynamic Memory Configuration register
A070 0104	MPMCDynamicRasCas0	Dynamic Memory RAS and CAS Delay
A070 0120	MPMCDynamicConfig1	Dynamic Memory Configuration register
A070 0124	MPMCDynamicRasCas1	Dynamic Memory RAS and CAS delay
A070 0140	MPMCDynamicConfig2	Dynamic Memory Configuration register
A070 0144	MPMCDynamicRasCas2	Dynamic Memory RAS and CAS delay
A070 0160	MPMCDynamicConfig3	Dynamic Memory Configuration register
A070 0164	MPMCDynamicRasCas3	Dynamic Memory RAS and CAS delay
A070 0200	MPMCStaticConfig0	Static Memory Configuration register
A070 0204	MPMCStaticWaitWen0	Static Memory Write Enable Delay
A070 0208	MPMCStaticWaitOen0	Static Memory Output Enable Delay
A070 020C	MPMCStaticWaitRd0	Static Memory Read Delay
A070 0210	MPMCStaticWaitPage0	Static Memory Page Mode Read Delay
A070 0214	MPMCStaticWaitWr0	Static Memory Write Delay
A070 0218	MPMCStaticWaitTurn0	Static Memory Turn Round Delay
A070 0220	MPMCStaticConfig1	Static Memory Configuration register
A070 0224	MPMCStaticWaitWen1	Static Memory Write Enable Delay
A070 0228	MPMCStaticWaitOen1	Static Memory Output Enable Delay
A070 022C	MPMCStaticWaitRd1	Static Memory Read Delay
A070 0230	MPMCStaticWaitPage1	Static Memory Page Mode Read Delay

Table 22: Memory Controller register map

Address	Register	Description
A070 0234	MPMCStaticWaitWr1	Static Memory Write Delay
A070 0238	MPMCStaticWaitTurn1	Static Memory Turn Round Delay
A070 0240	MPMCStaticConfig2	Static Memory Configuration register
A070 0244	MPMCStaticWaitWen2	Static Memory Write Enable Delay
A070 0248	MPMCStaticWaitOen2	Static Memory Output Enable Delay
A070 024C	MPMCStaticWaitRd2	Static Memory Read Delay
A070 0250	MPMCStaticWaitPage2	Static Memory Page Mode Read Delay
A070 0254	MPMCStaticWaitWr2	Static Memory Write Delay
A070 0258	MPMCStaticWaitTurn2	Static Memory Turn Round Delay
A070 0260	MPMCStaticConfig3	Static Memory Configuration register
A070 0264	MPMCStaticWaitWen3	Static Memory Write Enable Delay
A070 0268	MPMCStaticWaitOen3	Static Memory Output Enable Delay
A070 026C	MPMCStaticWaitRd3	Static Memory Read Delay
A070 0270	MPMCStaticWaitPage3	Static Memory Page Mode Read Delay
A070 0274	MPMCStaticWaitWr3	Static Memory Write Delay
A070 0278	MPMCStaticWaitTurn3	Static Memory Turn Round Delay
A070 0F00	MPMCITCR	Test Control register
A070 0F20	MPMCITIP	Test Input register
A070 0F40	MPMCITOP	Test Output register
A070 0FD0	MPMCPeriphID4	Peripheral Identification register bits [39:32]
A070 0FD4	MPMCPeriphID5	Reserved for Peripheral Identification register
A070 0FD8	MPMCPeriphID6	Reserved for Peripheral Identification register
A070 0FDC	MPMCPeriphID7	Reserved for Peripheral Identification register
A070 0FE0	MPMCPeriphID0	Peripheral Identification register bits [7:0]
A070 0FE4	MPMCPeriphID1	Peripheral Identification register bits [15:8]
A070 0FE8	MPMCPeriphID2	Peripheral Identification register bits [23:16]
A070 0FEC	MPMCPeriphID3	Peripheral Identification register bits [31:24]
A070 0FF0	MPMCPCellID0	Memory Controller Identification register bits[7:0]
A070 0FF4	MPMCPCellID1	Memory Controller Identification register bits [15:8]
A070 0FF8	MPMCPCellID2	Memory Controller Identification register bits [23:16]
A070 0FFC	MPMCPCellID3	Memory Controller Identification register bits {31:24]

Table 22: Memory Controller register map

Ethernet Control and Status registers

Address	Register	Description
A060 0000	EGCR1	Ethernet General Control Register #1
A060 0004	EGCR2	Ethernet General Control Register #2
A060 0008	EGSR	Ethernet General Status register
A060 000C	FIFORX	Ethernet RX FIFO Data register
A060 0010	FIFOTX	Ethernet TX FIFO Data register
A060 0014	FIFOTXS	Ethernet TX FIFO Status register
A060 0018	ETSR	Ethernet Transmit Status register
A060 001C	ERSR	Ethernet Receive Status register
A060 0400	MAC1	MAC Configuration Register #1
A060 0404	MAC2	MAC Configuration Register #2
A060 0408	IPGT	Back-to-Back Inter-Packet-Gap register
A060 040C	IPGR	Non-Back-to-Back Inter-Packet-Gap register
A060 0410	CLRT	Collision Window/Retry register
A060 0414	MAXF	Maximum Frame register
A060 0418	SUPP	PHY Support register
A060 041C	TEST	Test register
A060 0420	MCFG	MII Management Configuration register
A060 0424	MCMD	MII Management Command register
A060 0428	MADR	MII Management Address register
A060 042C	MWTD	MII Management Write Data register
A060 0430	MRDD	MII Management Read Data register
A060 0434	MIND	MII Management Indicators register
A060 0440	SA1	Station Address Register #1
A060 0444	SA2	Station Address Register #2
A060 0448	SA3	Station Address Register #3
A060 0500	SAFR	Station Address Filter register
A060 0504	HT1	Hash Table Register #1
A060 0508	HT2	Hash Table Register #2
A060 0680	STAT	Statistics Register Base (48 registers)
A060 0A00	RXAPTR	RX_A Buffer Descriptor Pointer register
A060 0A04	RXBPTR	RX_B Buffer Descriptor Pointer register

Table 23: Ethernet Control and Status register map

Address	Register	Description
A060 0A08	RXCPTR	RX_C Buffer Descriptor Pointer register
A060 0A0C	RXDPTR	RX_D Buffer Descriptor Pointer register
A060 0A10	EINTR	Ethernet Interrupt Status register
A060 0A14	EINTREN	Ethernet Interrupt Enable register
A060 0A18	TXPTR	TX Buffer Descriptor Pointer register
A060 0A1C	TXRPTR	TX Recover Buffer Descriptor Pointer register
A060 0A20	TXERBD	TX Error Buffer Descriptor Pointer register
A060 0A24	TXSPTR	TX Stall Buffer Descriptor Pointer register
A060 0A28	RXAOFF	RX_A Buffer Descriptor Pointer Offset register
A060 0A2C	RXBOFF	RX_B Buffer Descriptor Pointer Offset register
A060 0A30	RXCOFF	RX_C Buffer Descriptor Pointer Offset register
A060 0A34	RXDOFF	RX_D Buffer Descriptor Pointer Offset register
A060 0A38	TXOFF	Transmit Buffer Descriptor Pointer Offset register
A060 0A3C	RXFREE	RX Free Buffer register
A060 1000	TXBD	TX Buffer Descriptor RAM (256 locations)

Table 23: Ethernet Control and Status register map

PCI Configuration registers

Two registers are used to perform PCI configuration cycles, which allow access to PCI-to-AHB bridge configuration registers. The Configuration Address Port register (CONFIG_ADDR) is described in the following table. The Configuration Address Data Port register (CONFIG_DATA) does not have a specific format; it contains read or write configuration data.

Register	Description
A010 0000 – A01F FFFF	PCI Configuration Address Port register
A020 0000 – A02F FFFF	PCI Configuration Address Data Port register

Table 24: PCI Configuration register map

PCI Bridge Configuration registers

The PCI-to-AHB bridge supports these standard PCI configuration registers. The registers can be 8-, 16-, or 32-bits wide, as shown in the table.

Note: *Register number* refers to the REGISTER_NUMBER field in the Configuration Address Port register.

Register number	31:24	23:16	15:08	07:00
0x00	Device ID		Vendor ID	
0x01	Status		Command	
0x02	Class Code			Revision ID
0x03	BIST	Header	Latency timer	Cache size
0x04	Base address 0			
0x05	Base address 1			
0x06	Base address 2			
0x07	Base address 3			
0x08	Base address 4			
0x09	Base address 5			
0x0A	CardBus CIS pointer			
0x0B	Subsystem ID		Subsystem vendor ID	
0x0C	Expansion ROM			
0x0D	Reserved			
0x0E	Reserved			
0x0F	Max_Lat	Min_Gnt	Interrupt pin	Interrupt line

Table 25: PCI Bridge Configuration register map

PCI Arbiter Configuration registers

Address	Register	Description
A030 0000	PARBCFG	PCI Arbiter Configuration
A030 0004	PARBINT	PCI Arbiter Interrupt Status
A030 0008	PARBINTEN	PCI Arbiter Interrupt Enable
A030 000C	PMISC	PCI Miscellaneous Support
A030 0010	PCFG0	PCI Configuration 0
A030 0014	PCFG1	PCI Configuration 1
A030 0018	PCFG2	PCI Configuration 2
A030 001C	PCFG3	PCI Configuration 3
A030 0020	PAHBCFG	PCI Bridge Configuration
A030 0024	PAHBERR	PCI Bridge AHB Error Address
A030 0028	PCIERR	PCI Bridge PCI Error Address

Table 26: PCI Arbiter Configuration register map

Address	Register	Description
A030 002C	PINTR	PCI Bridge Interrupt Status
A030 0030	PINTEN	PCI Bridge Interrupt Enable
A030 0034	PALTMEM0	PCI Bridge AHB to PCI Memory Address Translate 0
A030 0038	PALTMEM1	PCI Bridge AHB to PCI Memory Address Translate 1
A030 003C	PALTIO	PCI Bridge AHB to PCI IO Address Translate
A030 0040	PMALT0	PCI Bridge PCI to AHB Memory Address Translate 0
A030 0044	PMALT1	PCI Bridge PCI to AHB Memory Address Translate 1
A030 0048	PALTCTL	PCI Bridge Address Translation Control
A030 004C	CMISC	CardBus Miscellaneous Support
A030 004C – A030 0FFC	N/A	Reserved (all read accesses return 0x0 value)
A030 1000	CSKTEV	CardBus Socket Event
A030 1004	CSKTMSK	CardBus Socket Mask
A030 1008	CSKTPST	CardBus Socket Present State
A030 100C	CSKTFEV	CardBus Socket Force Event
A030 1010	CSKTCTL	CardBus Socket Control
A030 1014 – A030 1FFC	N/A	Reserved (all read accesses return 0x0 value)

Table 26: PCI Arbiter Configuration register map

BBus Bridge Control and Status registers

Address	Description
A040 0000	DMA Channel 1 Buffer Descriptor Pointer
A040 0004	DMA Channel 1 Control register
A040 0008	DMA Channel 1 Status and Interrupt Enable
A040 0020	DMA Channel 2 Buffer Descriptor Pointer
A040 0024	DMA Channel 2 Control register
A040 0028	DMA Channel 2 Status and Interrupt Enable
A040 1000	BBus Bridge Interrupt Status
A040 1004	BBus Bridge Interrupt Enable

Table 27: BBus Bridge Control and Status register map

BBus DMA Control and Status registers

Address — DMA1 Address — DMA2	Description
9000 0000 9011 0000	DMA Channel 1 Buffer Descriptor Pointer
9000 0020 9011 0020	DMA Channel 2 Buffer Descriptor Pointer
9000 0040 9011 0040	DMA Channel 3 Buffer Descriptor Pointer
9000 0060 9011 0060	DMA Channel 4 Buffer Descriptor Pointer
9000 0080 9011 0080	DMA Channel 5 Buffer Descriptor Pointer
9000 00A0 9011 00A0	DMA Channel 6 Buffer Descriptor Pointer
9000 00C0 9011 00C0	DMA Channel 7 Buffer Descriptor Pointer
9000 00E0 9011 00E0	DMA Channel 8 Buffer Descriptor Pointer
9000 0100 9011 0100	DMA Channel 9 Buffer Descriptor Pointer
9000 0120 9011 0120	DMA Channel 10 Buffer Descriptor Pointer
9000 0140 9011 0140	DMA Channel 11 Buffer Descriptor Pointer
9000 0160 9011 0160	DMA Channel 12 Buffer Descriptor Pointer
9000 0180 9011 0180	DMA Channel 13 Buffer Descriptor Pointer
9000 01A0 9011 01A0	DMA Channel 14 Buffer Descriptor Pointer
9000 01C0 9011 01C0	DMA Channel 15 Buffer Descriptor Pointer
9000 01E0 9011 01E0	DMA Channel 16 Buffer Descriptor Pointer
9000 0010 9011 0010	DMA Channel 1 Control register

Table 28: BBus DMA Control and Status register map

Address — DMA1 Address — DMA2	Description
9000 0030 9011 0030	DMA Channel 2 Control register
9000 0050 9011 0050	DMA Channel 3 Control register
9000 0070 9011 0070	DMA Channel 4 Control register
9000 0090 9011 0090	DMA Channel 5 Control register
9000 00B0 9011 00B0	DMA Channel 6 Control register
9000 00D0 9011 00D0	DMA Channel 7 Control register
9000 00F0 9011 00F0	DMA Channel 8 Control register
9000 0110 9011 0110	DMA Channel 9 Control register
9000 0130 9011 0130	DMA Channel 10 Control register
9000 0150 9011 0150	DMA Channel 11 Control register
9000 0170 9011 0170	DMA Channel 12 Control register
9000 0190 9011 0190	DMA Channel 13 Control register
9000 01B0 9011 01B0	DMA Channel 14 Control register
9000 01D0 9011 01D0	DMA Channel 15 Control register
9000 01F0 9011 01F0	DMA Channel 16 Control register
9000 0014 9011 0014	DMA Channel 1 Status/Interrupt Enable register
9000 0034 9011 0034	DMA Channel 2 Status/Interrupt Enable register
9000 0054 9011 0054	DMA Channel 3 Status/Interrupt Enable register

Table 28: BBus DMA Control and Status register map

Address — DMA1 Address — DMA2	Description
9000 0074 9011 0074	DMA Channel 4 Status/Interrupt Enable register
9000 0094 9011 0094	DMA Channel 5 Status/Interrupt Enable register
9000 00B4 9011 00B4	DMA Channel 6 Status/Interrupt Enable register
9000 00D4 9011 00D4	DMA Channel 7 Status/Interrupt Enable register
9000 00F4 9011 00F4	DMA Channel 8 Status/Interrupt Enable register
9000 0114 9011 0114	DMA Channel 9 Status/Interrupt Enable register
9000 0134 9011 0134	DMA Channel 10 Status/Interrupt Enable register
9000 0154 9011 0154	DMA Channel 11 Status/Interrupt Enable register
9000 0174 9011 0174	DMA Channel 12 Status/Interrupt Enable register
9000 0194 9011 0194	DMA Channel 13 Status/Interrupt Enable register
9000 01B4 9011 01B4	DMA Channel 14 Status/Interrupt Enable register
9000 01D4 9011 01D4	DMA Channel 15 Status/Interrupt Enable register
9000 01F4 9011 01F4	DMA Channel 16 Status/Interrupt Enable register

Table 28: BBus DMA Control and Status register map

BBus Utility Control and Status registers

Address	Description
9060 0000	Master Reset register
9060 0004	BBus Utility Interrupt Status register
9060 0010	GPIO Configuration Register #1
9060 0014	GPIO Configuration Register #2

Table 29: BBus Utility Control and Status register map

Address	Description
9060 0018	GPIO Configuration Register #3
9060 001C	GPIO Configuration Register #4
9060 0020	GPIO Configuration Register #5
9060 0024	GPIO Configuration Register #6
9060 0028	GPIO Configuration Register #7
9060 0030	GPIO Control Register #1
9060 0034	GPIO Control Register #2
9060 0040	GPIO Status Register #1
9060 0044	GPIO Status Register #2
9060 0050	BBus Timeout register
9060 0060	BBus DMA Interrupt Status register
9060 0064	BBus DMA Interrupt Enable register
9060 0070	USB Configuration register
9060 0080	Endian Configuration register
9060 0090	ARM Wake-Up register

Table 29: BBus Utility Control and Status register map

I^2C

Address	Register	Description
9050 0000	TX_DATA_REG / CMD_REG (write) RX_DATA_REG / STATUS_REG (read)	Programming interface registers Command register / Interrupt Handling and Status register
9050 0004	Master Address register	Master device address, used to select a slave
9050 0008	Slave Address register	Slave device address
9050 000C	Configuration register	Setup Configuration register

Table 30: I^2C Control and Status registers

LCD Controller registers

Address	Register	Description
A080 0000	LCDTiming0	Horizontal axis panel control
A080 0004	LCDTiming1	Vertical axis panel control

Table 31: LCD Controller register map

Address	Register	Description
A080 0008	LCDTiming2	Clock and signal polarity control
A080 000C	LCDTiming3	Line end control
A080 0010	LCDUPBASE	Upper panel frame base address
A080 0014	LCDLPBASE	Lower panel frame base address
A080 0018	LCDINTRENABLE	Interrupt enable mask
A080 001C	LCDControl	LCD panel pixel parameters
A080 0020	LCDStatus	Raw interrupt status
A080 0024	LCDInterrupt	Final masked interrupts
A080 0028	LCDUPCURR	LCD upper panel current address value
A080 002C	LCDLPCURR	LCD lower panel current address value
A080 0030 – A080 01FC	Reserved	Reserved
A080 0200 – A080 03FC	LCDPalette	256 x 16-bit color palette

Table 31: LCD Controller register map

Serial Controller registers

The Serial Controller module contains four serial ports, referred to in this table as Channel 1, Channel 2, Channel 3, and Channel 4 respectively.

Address	Description
9020 0000	Channel 1 Control Register A
9020 0004	Channel 1 Control Register B
9020 0008	Channel 1 Status Register A
9020 000C	Channel 1 Bit-Rate register
9020 0010	Channel 1 FIFO Data register
9020 0014	Channel 1 Receive Buffer Timer
9020 0018	Channel 1 Receive Character Timer
9020 001C	Channel 1 Receive Match register
9020 0020	Channel 1 Receive Match Mask register
9020 0024	Channel 1 Control Register C
9020 0028	Channel 1 Status Register B
9020 002C	Channel 1 Status Register C
9020 0030	Channel 1 FIFO Data Last register

Table 32: Serial Controller register map

Address	Description
9020 0034	Channel 1 Flow Control
9020 0038	Channel 1 Transmit Override
9020 0040	Channel 2 Control Register A
9020 0044	Channel 2 Control Register B
9020 0048	Channel 2 Status Register A
9020 004C	Channel 2 Bit-Rate register
9020 0050	Channel 2 FIFO Data register
9020 0054	Channel 2 Receive Buffer Timer
9020 0058	Channel 2 Receive Character Timer
9020 005C	Channel 2 Receive Match register
9020 0060	Channel 2 Receive Match Mask Register
9020 0064	Channel 2 Control Register C
9020 0068	Channel 2 Status Register B
9020 006C	Channel 2 Status Register C
9020 0070	Channel 2 FIFO Data Last register
9020 0074	Channel 2 Flow Control
9020 0078	Channel 2 Transmit Override
9030 0000	Channel 3 Control Register A
9030 0004	Channel 3 Control Register B
9030 0008	Channel 3 Status Register A
9030 000C	Channel 3 Bit-Rate register
9030 0010	Channel 3 FIFO Data register
9030 0014	Channel 3 Receive Buffer Timer
9030 0018	Channel 3 Receive Character Timer
9030 001C	Channel 3 Receive Match register
9030 0020	Channel 3 Receive Match Mask register
9030 0024	Channel 3 Control Register C
9030 0028	Channel 3 Status Register B
9030 002C	Channel 3 Status Register C
9030 0030	Channel 3 FIFO Data Last register
9030 0034	Channel 3 Flow Control
9030 0038	Channel 3 Transmit Override

Table 32: Serial Controller register map

Address	Description
9030 0040	Channel 4 Control Register A
9030 0044	Channel 4 Control Register B
9030 0048	Channel 4 Status Register A
9030 004C	Channel 4 Bit-Rate register
9030 0050	Channel 4 FIFO Data register
9030 0054	Channel 4 Receive Buffer Timer
9030 0058	Channel 4 Receive Character Timer
9030 005C	Channel 4 Receive Match register
9030 0060	Channel 4 Receive Match Mask register
9030 0064	Channel 4 Control Register C
9030 0068	Channel 4 Status Register B
9030 006C	Channel 4 Status Register C
9030 0070	Channel 4 FIFO Data Last register
9030 0074	Channel 4 Flow Control
9030 0078	Channel 4 Transmit Override

Table 32: Serial Controller register map

IEEE 1284 Peripheral Controller registers

Address	Register	Description
9040 0000	GenConfig	General Configuration register
9040 0004	InterruptStatusandControl	Interrupt Status and Control register
9040 0008	FIFO Status	FIFO Status register
9040 000C	FwCmdFifoReadReg	Forward Command FIFO Read register
9040 0010	FwDatFifoReadReg	Forward Data FIFO Read register
9040 0014	RvCmdFifoWriteReg	Reverse Command FIFO Write register
9040 0018	RvCmdFifoWriteReg – Last	Reverse Command FIFO Write Register — Last
9040 001C	RvDatFifoWriteReg	Reverse Data FIFO Write register
9040 0020	RvDatFifoWriteReg – Last	Reverse Data FIFO Write Register — Last
9040 0024	FwCmdDmaControl	Forward Command DMA Control register
9040 0028	FwDatDmaControl	Forward Data DMA Control register
9040 002C – 9040 00FC	Reserved (no ACK)	N/A

Table 33: IEEE 1284 Peripheral Controller rgister map

Address	Register	Description
9040 0100 – 9040 017C CSRs (8-bit wide)		
9040 0100	PD	Printer Data Pins register
9040 0104	PSR	Port Pin Status register (host)
9040 0108	PCR	Port Control register
9040 010C	PIN	Port Pin Status register (peripheral)
9040 0110	FFX	Forward Buffer Read Data register
9040 0114	FEA	Feature Control Register A
9040 0118	FEB	Feature Control Register B
9040 011C	FEI	Interrupt Enable register
9040 0120	FEM	Master Enable register
9040 0124	EXR	Extensibility Byte Requested by Master
9040 0128	ECR	Extended Control register
9040 012C	STI	Interrupt Status register
9040 0130	TOC	Interrupt Timeout Counter
9040 0134	MSK	Mask Pin Interrupt
9040 0138	PIT	Pin Interrupt Control
9040 013C	RFX	Reverse Buffer Data
9040 0140 – 9040 0164	Reserved	N/A
9040 0168	GRN	Granularity Value
9040 016C	SFX	Buffer Full Status
9040 0170 – 9040 0174	Reserved	N/A
9040 0178	PHA	Core Phase register

Table 33: IEEE 1284 Peripheral Controller rgister map

USB Configuration registers

Note: USB device DMA registers are listed in "BBus DMA Control and Status registers" on page 45.

Register	Description
9010 0000	Global Control/Status register
9010 0004	Device Control/Status register
9010 0008	Host Control/Status register
9010 000C	Global Interrupt Enable
9010 0010	Global Interrupt Status
9010 1000	HcRevision register
9010 1004	HcControl register
9010 1008	HcCommandStatus register
9010 100C	HcInterruptStatus register
9010 1010	HcInterruptEnable register
9010 1014	HcInterruptDisable register
9010 1018	HcHCCA (Host Controller Communications Area) register
9010 101C	HcCurrentPeriodED register (ED = Endpoint Descriptor)
9010 1020	HcControlHeadED register
9010 1024	HcControlCurrentED register
9010 1028	HcBulkHeadED register
9010 102C	HcBulkCurrentED register
9010 1030	HcDoneHead register
9010 1034	HcFmInterval register (Fm = Frame)
9010 1038	HcFmRemaining register
9010 103C	HcFmNumber register
9010 1040	HcPeriodicStart register
9010 1044	HcLSThreshold register
9010 1048	HcRhDescriptorA register (Rh = Root hub)
9010 104C	HcRhDescriptorB register
9010 50	HcRhStatus register
9010 1054	HcRhPortStatus[1]
9010 2000	Device Descriptor/Setup Command register
9010 2004	Physical Endpoint Descriptor #1
9010 2008	Physical Endpoint Descriptor #2

Table 34: USB Configuration register map

Register	Description
9010 200C	Physical Endpoint Descriptor #3
9010 2010	Physical Endpoint Descriptor #4
9010 2014	Physical Endpoint Descriptor #5
9010 2018	Physical Endpoint Descriptor #6
9010 201C	Physical Endpoint Descriptor #7
9010 2020	Physical Endpoint Descriptor #8
9010 2024	Physical Endpoint Descriptor #9
9010 2028	Physical Endpoint Descriptor #10
9010 202C	Physical Endpoint Descriptor #11
9010 2030	Physical Endpoint Descriptor #12
9010 2034	Configuration Descriptor #1
9010 2038	Configuration Descriptor #2
9010 203C	Configuration Descriptor #3
9010 2040	Configuration Descriptor #4
9010 2044	Configuration Descriptor #5
9010 3000	FIFO Interrupt Status 0
9010 3004	FIFO Interrupt Enable 0
9010 3010	FIFO Interrupt Status 1
9010 3014	FIFO Interrupt Enable 1
9010 3020	FIFO Interrupt Status 2
9010 3024	FIFO Interrupt Enable 2
9010 3030	FIFO Interrupt Status 3
9010 3030	FIFO Interrupt Enable 3
9010 3080	FIFO Packet Control #1
9010 3084	FIFO Packet Control #2
9010 3088	FIFO Packet Control #3
9010 308C	FIFO Packet Control #4
9010 3094	FIFO Packet Control #5
9010 3094	FIFO Packet Control #6
9010 3098	FIFO Packet Control #7
9010 309C	FIFO Packet Control #8
9010 30A0	FIFO Packet Control #9

Table 34: USB Configuration register map

Register	Description
9010 30A4	FIFO Packet Control #10
9010 30A8	FIFO Packet Control #11
9010 30AC	FIFO Packet Control #12
9010 30B0	FIFO Packet Control #13
9010 3100	FIFO Status and Control #1
9010 3108	FIFO Status and Control #2
9010 3110	FIFO Status and Control #3
9010 3118	FIFO Status and Control #4
9010 3120	FIFO Status and Control #5
9010 3128	FIFO Status and Control #6
9010 3130	FIFO Status and Control #7
9010 3138	FIFO Status and Control #8
9010 3140	FIFO Status and Control #9
9010 3148	FIFO Status and Control #10
9010 3150	FIFO Status and Control #11
9010 3158	FIFO Status and Control #12
9010 3160	FIFO Status and Control #13
9010 3104	FIFO Data #1
9010 310C	FIFO Data #2
9010 3114	FIFO Data #3
9010 311C	FIFO Data #4
9010 3124	FIFO Data #5
9010 312C	FIFO Data #6
9010 3134	FIFO Data #7
9010 313C	FIFO Data #8
9010 3144	FIFO Data #9
9010 314C	FIFO Data #10
9010 3154	FIFO Data #11
9010 315C	FIFO Data #12
9010 3164	FIFO Data #13

Table 34: USB Configuration register map

Electrical characteristics

The NS9750 operates at a 1.5V core, with 3.3V I/O ring voltages.

Absolute maximum ratings

Permanent device damage can occur if the absolute maximum ratings are exceeded even for an instant.

Parameter	Symbol†	Rating	Unit
DC supply voltage	V_{DDA}	-0.3 to +3.9	V
DC input voltage	V_{INA}	-0.3 to V_{DDA} + 0.3	V
DC output voltage	V_{OUTA}	-0.3 to V_{DDA} + 0.3	V
DC input current	I_{IN}	±10	mA
Storage temperature	T_{STG}	-40 to +125	°C
† V_{DDA}, V_{INA}, V_{OUTA}: Ratings of I/O cells for 3.3V interface			

Recommended operating conditions

Recommended operating conditions specify voltage and temperature ranges over which a circuit's correct logic function is guaranteed. The specified DC electrical characteristics (see "DC electrical characteristics" on page 58) are satisfied over these ranges.

Parameter	Symbol†	Rating	Unit
DC supply voltage	V_{DDA}	3.0 to 3.6	V
	V_{DDC}	1.4 to 1.6	V
Maximum junction temperature	T_j	125	°C
† V_{DDA}: Ratings of I/O cells for 3.3V interface V_{DDC}: Ratings of internal cells			

Maximum power dissipation

Table 35 shows the maximum power dissipation, including sleep mode information, for I/O and core:

	Operation			Sleep mode with wake up on			
CPU clock	Full	No PCI	No PCI, LCD	All ports	BBus ports	AHB bus ports	No wake up ports
Total @ 200 MHz	1.7 W	1.55 W	1.5 W	350 mW	285 mW	240 mW	180 mW
Core	1.05 W	1 W	1 W	260mW	210 mW	220 mW	170 mW
I/O	0.65 W	0.55 W	0.5 W	90 mW	75 mW	20 mW	10 mW
Total @ 162 MHz	1.4 W	1.25 W	1.2 W	285 mW	235 mW	200 mW	145 mW
Core	0.9 W	0.8 W	0.8 W	210 mW	170 mW	180 mW	140 mW
I/O	0.5 W	0.45 W	0.4 W	75 mW	65 mW	20 mW	5 mW
Total @ 125 MHz	1.05 W	1 W	950 mW	220 mW	180 mW	150 mW	110 mW
Core	0.65 W	0.65 W	640 mW	160 mW	130 mW	140 mW	105 mW
I/O	0.4 W	0.35 W	310 mW	60 mW	50 mW	10 mW	5 mW

Table 35: Mercury power dissipation

DC electrical characteristics

DC electrical characteristics specify the worst-case DC electrical performance of the I/O buffers that are guaranteed over the specified temperature range.

Inputs

All electrical inputs are 3.3V interface.

Note: V_{SS} = 0V (GND)

Sym	Parameter	Condition	Value		Unit
V_{IH}	High-level input voltage: LVTTL level PCI level		Min	 2.0 $0.5V_{DDA}$	 V V
V_{IL}	Low-level input voltage: LVTTL level PCI level		Max	 0.8 $0.3V_{DDA}$	 V V
I_{IH}	High-level input current (no pulldown) Input buffer with pulldown	$V_{INA} = V_{DDA}$	Min/Max Min/Max	-10/10 10/200	µA µA
I_{IL}	Low-level input current (no pullup) Input buffer with pullup	$V_{INA} = V_{SS}$	Min/Max Min/Max	-10/10 10/200	µA µA
IOZ	High-impedance leakage current	$V_{OUTA} = V_{DDA}$ or V_{SS}	Min/Max	-10/10	µA
IDDS	Quiescent supply current	$V_{INA} = V_{DDA}$ or V_{SS}	Max	TBD	

Outputs

All electrical outputs are 3.3V interface.

Sym	Parameter	Value		Unit
V_{OH}	High-level output voltage (LVTTL)	Min	V_{DDA}-0.6	V
V_{OL}	Low-level output voltage (LVTTL)	Max	0.4	V
V_{OH}	PCI high-level output voltage	Min	$0.9V_{DDA}$	V
V_{OL}	PCI low-level output voltage	Max	$0.1V_{DDA}$	V

Power sequencing

All of the 3.3V and 1.5V power should be applied and removed within 100 milliseconds to prevent parasitic devices from experiencing transient overlap currents for long periods of time. Overlap currents, if allowed to continue flowing unchecked, not only increase total power dissipation in a circuit but degrade the circuit reliability, shortening the circuit's usual operating life. An increase in overlap currents occurs in these situations:

- When power supplies are not applied or removed simultaneously.
- When any one of the power supplies is removed suddenly.

AC Characteristics

This section provides the AC characteristics, or timing specifications, integral to the operation of the NS9750.

Memory controller timing diagrams

Table 36 describes the values shown in the memory controller SDRAM timing diagrams (Figure 6, Figure 7, Figure 8, and Figure 9).

Parameter	Description	Value
T1	row/column address to clk_out setup time	6 ns
T2	bank address to clk_out setup time	6 ns
T3	dy_cs_n to clk_out setup time	6 ns
T4	ras_n to clk_out setup time	6 ns
T5	cas_n to clk_out setup time	6 ns
T6	data_mask to clk_out setup time	6 ns
T7	write data to clk_out setup time	6 ns
T8	we_n to clk_out setup time	6 ns
T9	read data access time	5.4 ns
T10	row/column address to clk_out setup time	2.5 ns
T11	bank address to clk_out setup time	2.5 ns
T12	dy_cs_n to clk_out setup time	2.5 ns
T13	ras_n to clk_out setup time	2.5 ns
T14	cas_n to clk_out setup time	2.5 ns
T15	data_mask to clk_out setup time	2.5 ns
T16	write data to clk_out setup time	2.5 ns
T17	we_n to clk_out setup time	2.5 ns
T18	read data access time	5.4 ns

Table 36: Memory controller: SDRAM timing parameters

sdram_read_cmd_dly

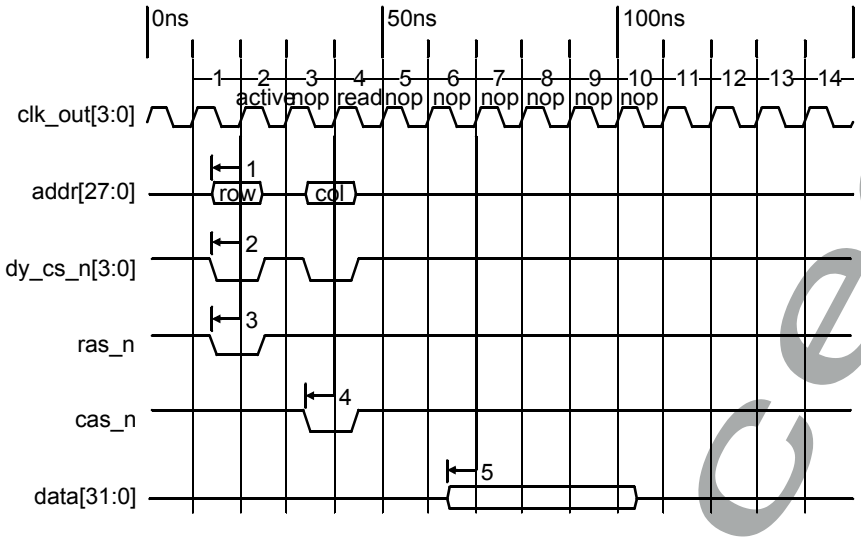


Figure 6: SDRAM read: command out delayed, cas latency = 3

Notes:

1 Timing parameters 1 through 4 are the same: 2.5ns setup.

2 Timing parameter 5 shows a PC133 access time of 5.4ns.

sdram_read_clk_dly

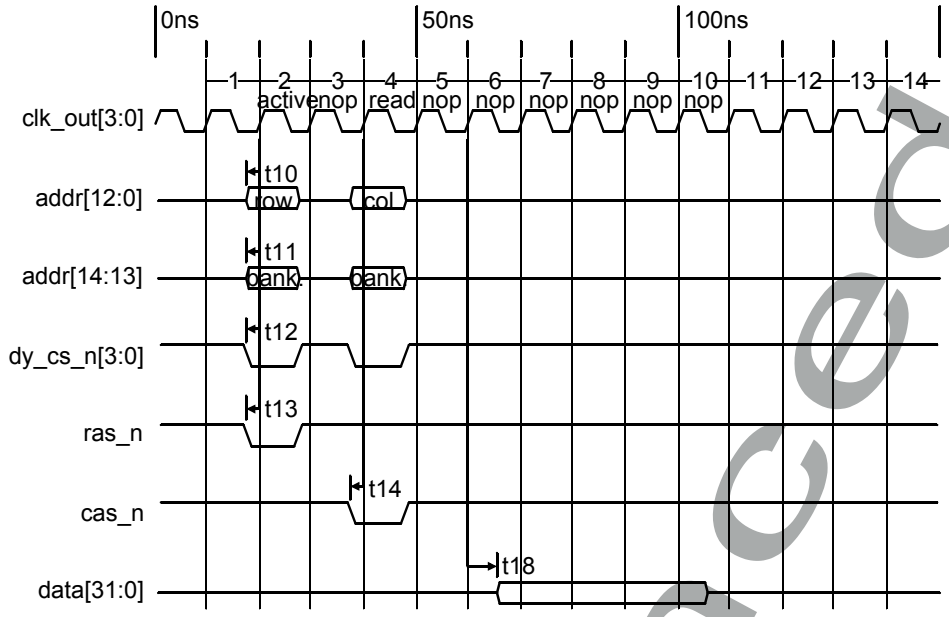


Figure 7: SDRAM read: clock out delayed, cas latency = 3

Notes:

1 Timing parameters t10 through t14 are the same: 2.5ns setup.

2 Timing parameter t18 shows a PC133 access time of 5.4ns.

sdram_write_cmd_dly

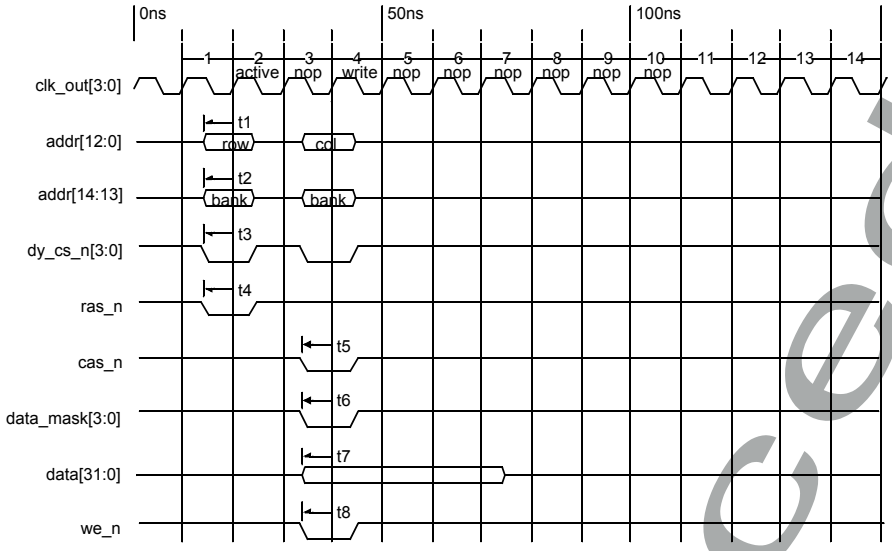


Figure 8: SDRAM write: command out delayed, cas latency = 3

Notes:

1 Port size determines which data mask signals are active:
   - 8-bit port = data_mask[0]
   - 16-bit port = data_mask[1:0]
   - 32-bit port = data_mask[3:0]

2 All of the timing parameters in this timing diagram are the same: 6ns setup.

sdram_write_clk_dly

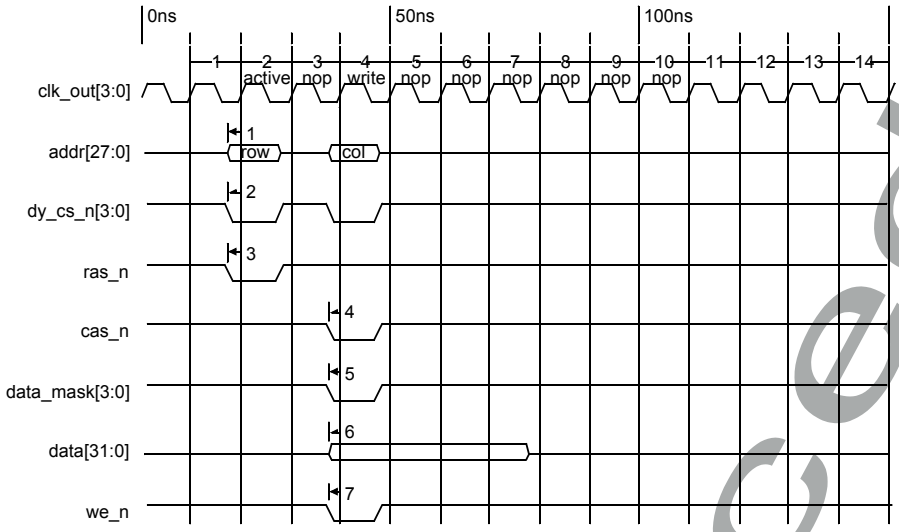


Figure 9: SDRAM write: clock out delayed, cas latency = 3

Notes:

1 Port size determines which data mask signals are active:
   - 8-bit port = data_mask[0]
   - 16-bit port = data_mask[1:0]
   - 32-bit port = data mask[3:0]

2 All of the timing parameters in this timing diagram are the same: 2.5 ns setup.

Table 37 describes the values shown in the memory controller SRAM timing diagrams (Figure 10 and Figure 11).

Parameter	Description	Value
T1	address to clk_out setup time	6 ns
T2	byte_lane_sel_n to clk_out setup time	6 ns
T3	st_cs_n to clk_out setup time	6 ns
T4	read data to clk_out setup time	tbd ns
T5	st_oe_n to clk_setup time	6 ns
T6	write data to clk_out setup time	6 ns
T7	we_n to clk_out setup time	6 ns

Table 37: Memory controller: SRAM timing parameters

sram_read

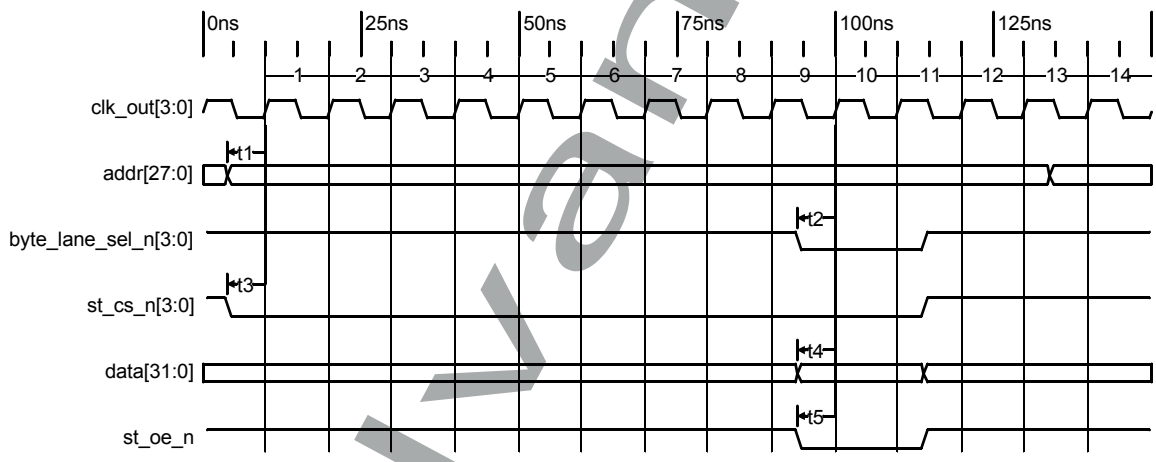


Figure 10: SRAM read timing parameters

Notes:

1 st_cs_n assert to st_oe_n assert delay is programmed to 9 clkout cycles.

2 st_cs_n assert to st_oe_n deassert delay is programmed to 11 clkout cycles.

3 Port size determines which byte enable signals are active:
- 8-bit port = byte_lane_sel_n[0]
- 16-bit port = byte_lane_sel_n[1:0]
- 32-bit port = byte_lane_sel_n[3:0]

sram_write

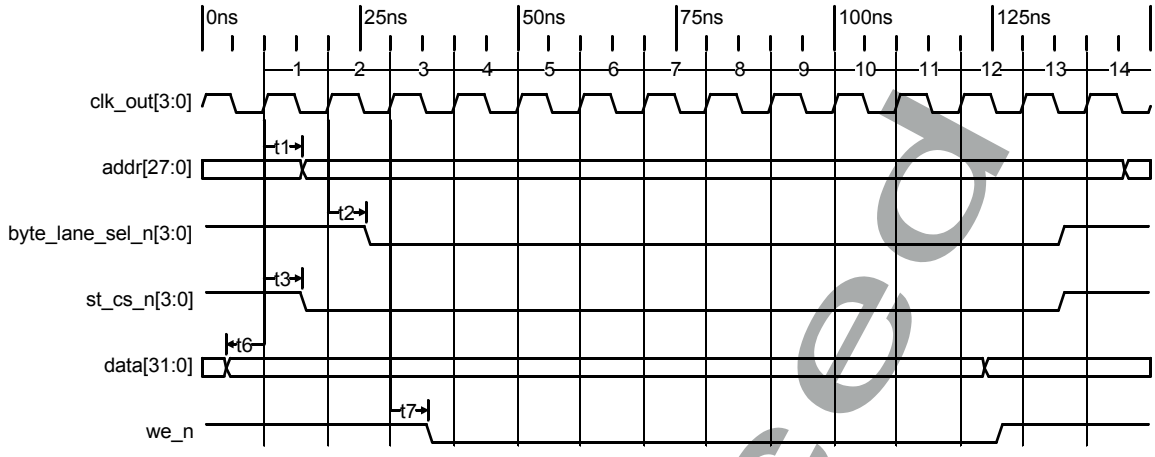


Figure 11: SRAM write timing parameters

Notes:

1 st_cs_n assert to we_n assert delay is programmed to 2 clkout cycles.

2 st_cs_n assert to we_n deassert delay is programmed to 11 clkout cycles.

3 Port size determines which byte enable signals are active:
- 8-bit port = byte_lane_select[0]
- 16-bit port = byte_lane_select[1:0]
- 32-bit port = byte_lane_select[3:0]

Reset timing diagram

Table 38 describes the values shown in the Reset timing diagram. Figure 12 shows the timing diagram.

Parameter	Description	Value
T1	reset_n minimum time after powerup	10 x1_sys_osc clock cycles
T2	reset_n to reset_done time	4 ms

Table 38: Reset timing parameters

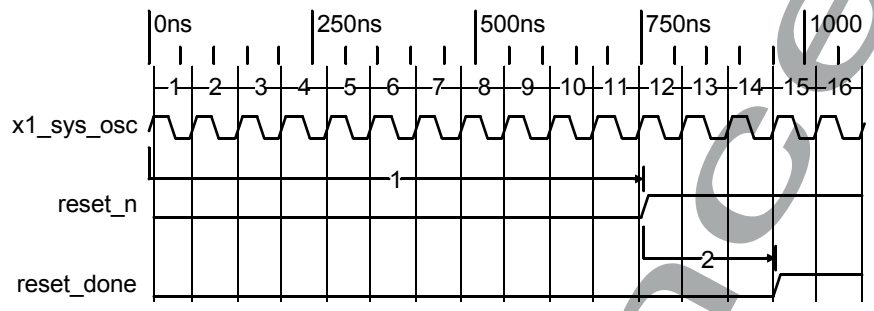


Figure 12: Reset timing diagram

Notes:

1 t1: reset_n must be held low for a minimum of 10 x1_sys_osc clock cycles after power up.

2 t2: reset_done is asserted 4ms after reset_n is driven high.

3 The hardware strapping pins are latched when reset_done is asserted.

LCD controller timing diagrams

Table 39 describes the values shown in the LCD controller timing diagrams (Figure 13, Figure 14, Figure 15, and Figure 16).

Parameter	Description	Register	Value	Units
T1	Horizontal front porch blanking	LCDTiming0	HFP + 1	CLCP periods
T2	Horizontal sync width	LCDTiming0	HSW + 1	CLCP periods
T3	Horizontal period	N/A	T1 + T2 + T3 + T4	CLCP periods
T4	Horizontal back porch	LCDTiming0	HBP + 1	CLCP periods
T5	TFT active line	LCDTiming0	16 * (PPL + 1) (see note 3)	CLCP periods
T6	LCD panel clock frequency	LCDTiming2	For BCD = 0: CLCDCLK/(PCD + 2) For BCD = 1: CLCDCLK (see note 1)	MHz
T7	TFT vertical sync width	LCDTiming1	VSW + 1	H lines
T8	TFT vertical lines/frame	N/A	T7 + T9 + T10 + T11	H lines
T9	TFT vertical back porch	LCDTiming1	VBP	H lines
T10	TFT vertical front porch	LCDTiming1	VFP	H lines
T11	Active lines/frames	LCDTiming1	LPP + 1	H lines
T12	STN HSYNC inactive to VSYNC active	LCDTiming0	HBP + 1	CLCP periods
T13	STN vertical sync width	N/A	1	H lines
T14	STN vertical lines/frames	N/A	T11 + T16	H lines
T15	STN active line	LCDTiming2	CPL + 1 (see note 4)	CLCP periods
T16	STN vertical blanking	LCDTiming1	VSW + VFP + VBP + 1	H lines

Table 39: LCD controller timing parameters

Notes:

1 CLCDCLK is selected from one of five possible sources:
- lcdclk/2 (lcdclk is an external oscillator)
- AHB clock
- AHB clock/2
- AHB clock/4
- AHB clock/8

2 The polarity of CLLP, CLFP, CLCP, and CLAC can be inverted using control fields in the LCDTiming1 register.

3 The CPL (clocks per line) field in the LCDTiming2 register must be programmed to T5-1.

4 The PPL (pixels per line) field in the LCDTiming0 register must also be programmed correctly.

5 The following data widths are supported:
- 4-bit mono STN single panel
- 8-bit mono STN single panel
- 8-bit color STN single panel
- 4-bit mono STN dual panel (8 bits to LCD panel)
- 8-bit mono STN dual panel (16 bits to LCD panel)
- 8-bit color STN dual panel (16 bits to LCD panel)
- 24-bit TFT
- 18-bit TFT

6 See the *Mercury Hardware Reference* for bit field definitions in the LCDTiming [0, 1, 2] registers.

lcd_stn_data

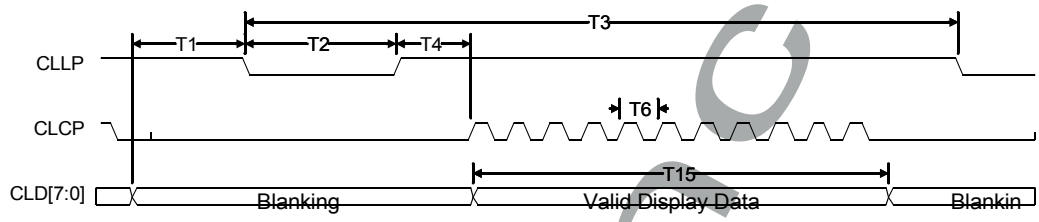


Figure 13: Horizontal timing parameters for STN displays

lcd_stn_sync

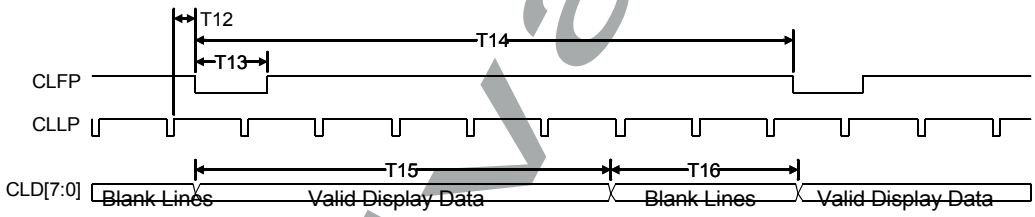


Figure 14: Vertical timing parameters for STN displays

lcd_tft_data

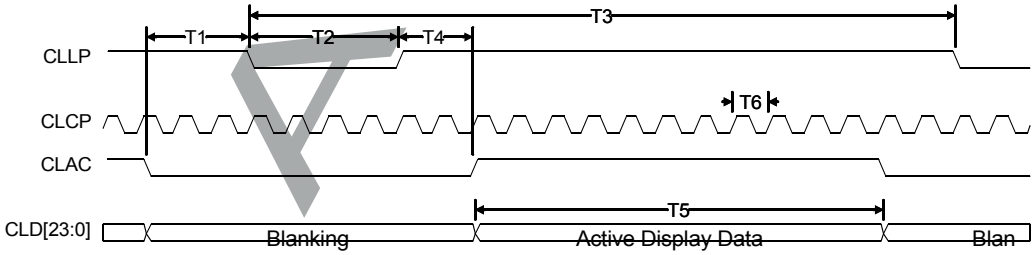


Figure 15: Horizontal timing parameters for TFT displays

lcd_tft_sync

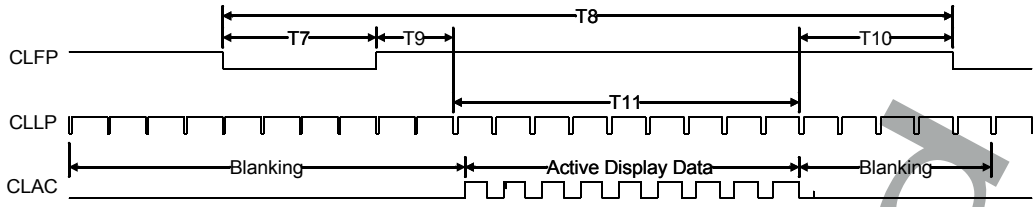


Figure 16: Vertical timing parameters for TFT displays

Power supply

Please contact the factory for proposed schematics.

Packaging

The NS9750 dimensions and pinout are shown in the next two diagrams.

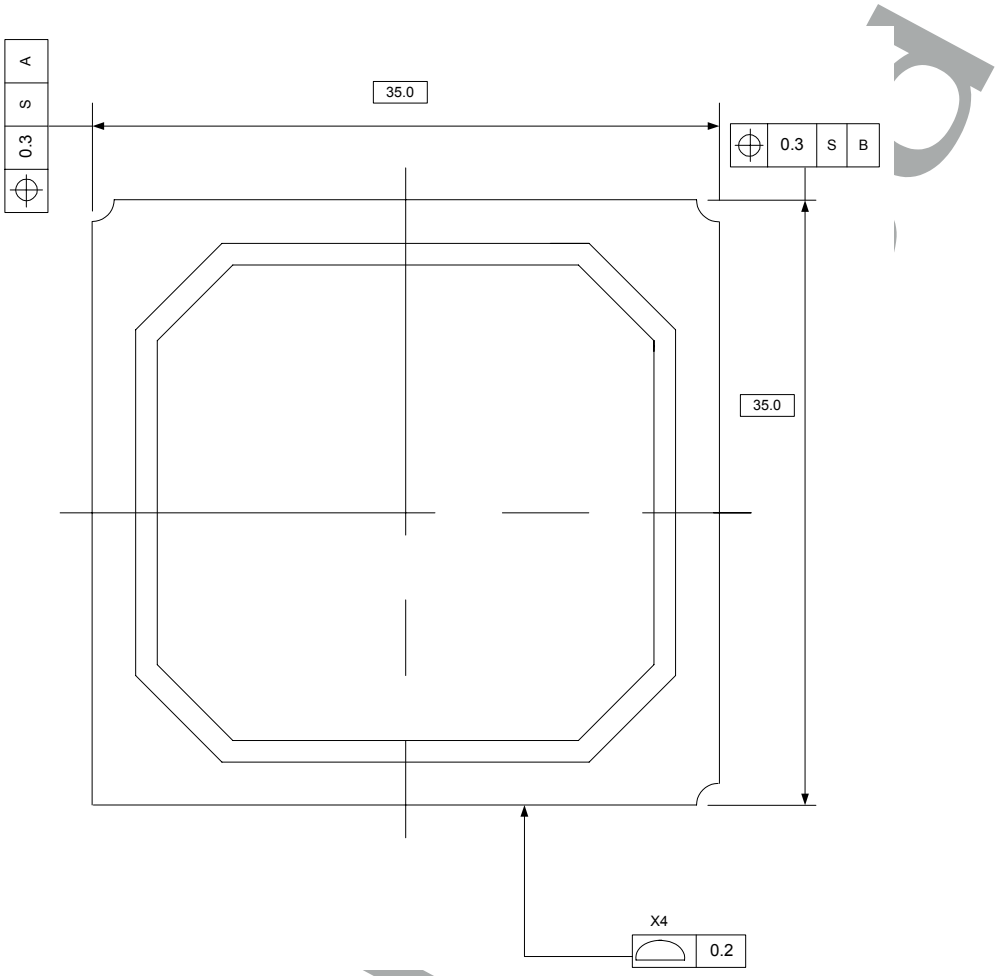


Figure 17: NS9750 top view

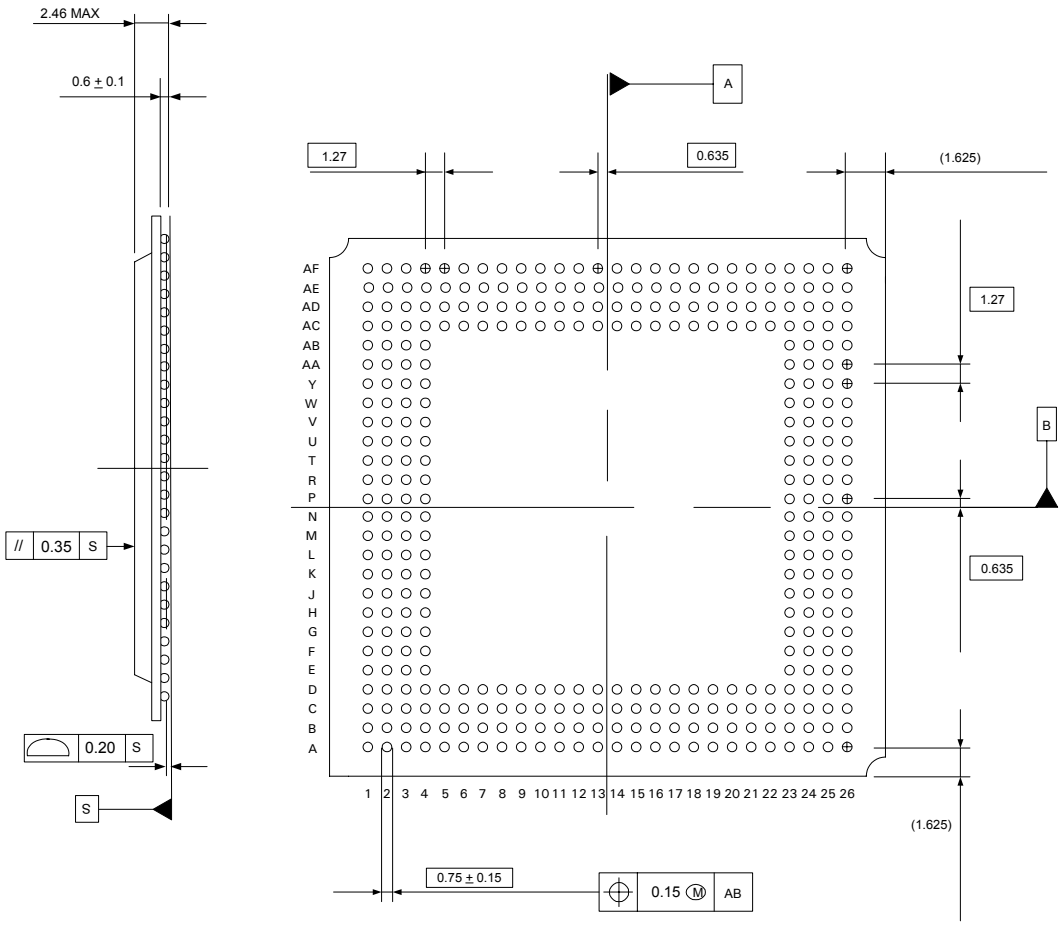


Figure 18: NS9750 bottom and side view

Part ordering information

TBD

P/N: 91001206 A

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